# MODELING, DESIGN, FABRICATION AND DEMONSTRATION OF ULTRA-THIN, HIGH-PERFORMANCE GLASS PANEL EMBEDDED (GPE) PACKAGES FOR MM-WAVE APPLICATIONS

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# MODELING, DESIGN, FABRICATION AND DEMONSTRATION OF ULTRA-THIN, HIGH-PERFORMANCE GLASS PANEL EMBEDDED (GPE) PACKAGES FOR MM-WAVE APPLICATIONS

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# SUMMARY

The objective of the proposed research is to model, design, fabricate and demonstrate ultra-thin, high-performance ultra-thin glass panel embedded package (GPE) for mm-Wave applications. Ultra-thin low-warpage GPE packages were demonstrated with thickness less than 150 μm applying advanced low-cost large panel based double side carrier process. Low-loss interconnects were modeled and designed with interconnection loss below 0.2 dB at 77 GHz enabled by ultra-low loss dielectric, and high precision processing with minimal variations in line and via geometries on glass substrates. A die-package codesign was proposed for high-frequency characterization of ultra-thin GPE package for mm-Wave applications.

# CHAPTER 1. INTRODUCTION

## 1.1 What is Embedding and Fan-out Packaging?

Embedding and Fan-out packaging are two different technologies. All the single-chip packaging technologies can be classified into four types, as shown in Fig. 1: a) Wafer-level Packaging b) Embedded Packaging c) Fan-out Packaging and d) Embedded and Fan-out Packaging.

Wafer level packaging (WLP) is emerging as a strategic and dominant packaging technology because of its merits and available manufacturing infrastructure over traditional packaging. WLP started in the 1990's by depositing a set of redistributing wiring layers on wafers in the wafer fab, placing bumps to form Input/Outputs (I/Os), followed by singulating the packaged ICs and finally making the WLP ready for board assembly. All WLPs are chip-scale packages (CSPs), which means the chip and package sizes are nearly the same. This is the best package electrically; however, WLP is limited to small ICs and to small packages, typically below 6 mm x 6 mm.

Fan-out packages provide more I/Os to connect to the board by extending the chip size by molding and is very important for many applications, particularly for packaging processor chips for computing applications. The fan-out means fanning out of I/Os beyond the footprint of the IC in the package. Fan-out technology, by itself, is not new; in fact, most of billions of packages, since the 1970s, are manufactured annually as fan-out packages. However, it is new for wafer level packages that are manufactured in the wafer fabs. Since wafer level packages are small and therefore limited in board level I/Os, wafer fan-out

allows more I/Os by fanning out the wafer level package and in doing so, it eliminates the board-level I/O limitation of WLPs. c), a Ball Grid Array (BGA) package, one of the more recent packages, is an example of a Fan-out package. These are manufactured, however, not in the wafer fab from round wafers, but as strips, panels or boards in package and board foundries.

Embedding technology is a different technology than wafer level packaging to address a set of different needs. Embedding means embedding the chip inside the substrate package or board with building up of RDL wiring layers on top of the chips. For this reason, it is also called chip-first. In this technology, RDL wiring is directly deposited on reconstituted ICs into 200 or 300 mm round wafers by molding them with epoxy molding compounds. Therefore, the interconnections between the chip and package or board are very short; there is no assembly of chips and if the chip is ground from its original 750 μm thickness to about 30-100 μm, the embedded package becomes ultra-miniaturized. Some applications such as power and RF benefit from this approach even if they do not require more I/Os at chip- and board- levels. Fan-out and embedding technologies, therefore, are two different technologies with two different goals. But they can be combined at wafer-level in the wafer foundry as Fan-Out Wafer Level Package (FO-WLP) or at panel-level in the package foundry as Panel Level Package (PLP). Such a concept is illustrated in Figure 1 d). These technologies when combined have many applications that include digital, RF and millimeter wave, low power and high power.

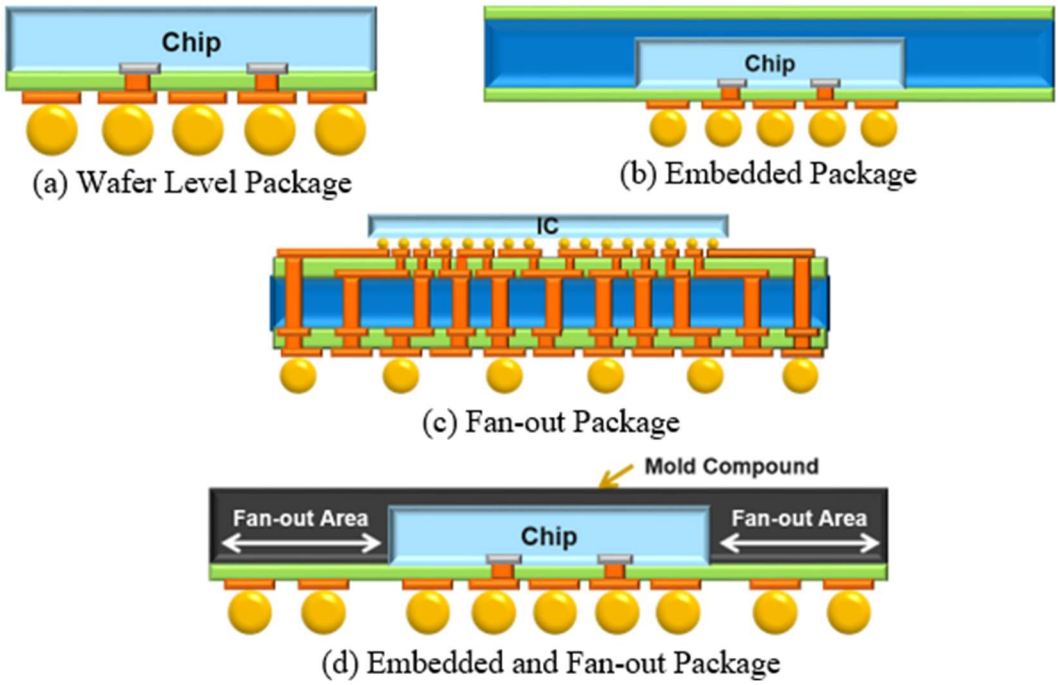



**Figure 1. Four types of packages: (a) wafer-level package (WLP), b) embedded package, (c) fan-out package, and (d) embedded and fan-out package.**

### 1.2 What is mm-Wave/5G?

Millimeter wave (MM wave), also known as millimeter band, is the band of spectrum with wavelengths between 10 millimeters and 1 millimeter, while RF is between 30GHz (wavelength 10mm) and 300GHz (wavelength 1mm).

5G is the 5th generation mobile network. It is a new global wireless standard after 1G, 2G, 3G, and 4G networks. 5G wireless technology is meant to deliver higher multi-Gbps peak data speeds with ultra low latency, more reliability, massive network capacity, increased availability, and a more uniform user experience to more users.

MmWave and 5G are used almost synonymously, but there are key differences between the two. The mmWave technology is just one part of what future 5G networks will use.

The frequency spectrum of 5G and mmWave is shown in Figure 2. Millimeter wave has numerous uses, including telecommunications, short-range RADAR and airport security scanners. In telecommunications, it is used for high-bandwidth WLANs and short-range personal area networks (PANs). Its high bandwidth capacity is ideal for applications like short-distance wireless transmission of ultra-high definition video and communications from small, low-power IoT devices. The limited propagation distance, small cell size and high data rates make millimeter wave ideal for communications between autonomous vehicles.

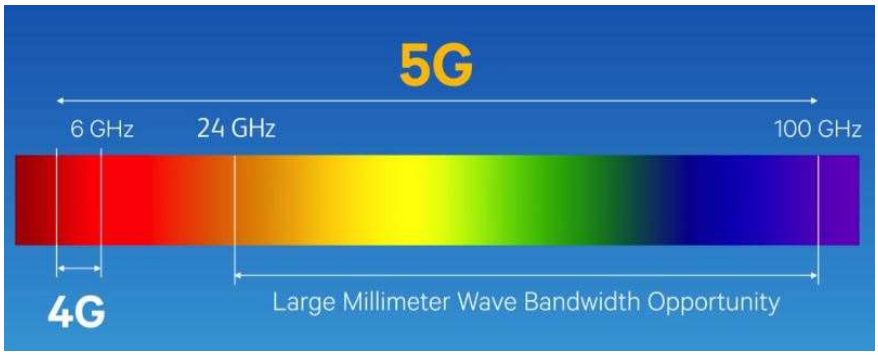



**Figure 2. Frequency spectrum of 5G and mmWave**

### 1.3 Strategic Need

The increasing demands for performance, functionality, miniaturization, reliability and cost of millimeter-wave systems have been driving many advances in packaging technologies for mm-wave applications. Wire-bonding was used to connect the semiconductor chips to the RF substrate traditionally, which is then assembled onto the PCB. However, the electrical parasitic of such a bonded wire severely affect the performance, with the tolerances varying as much as ± 15% [1]. Flip-chip technology, emerged as an improved alternative to wire-bonding, delivered better RF performance with

reduced radiation losses and improved impedance matching due to smaller electrical length. The insertion loss with flip-chip packages can be less than 0.2 dB [2] compared to nearly 2 dB loss with the wire-bonding technology [3]. The embedded wafer level ball grid array (eWLB) was the next major advance in package technology, which was first reported-manufactured by Infineon in 2006 [4]. This enabled better electrical performance at millimeter-wave frequencies along with reduced package size and the flexibility of antenna integration directly in the eWLB package, instead of the integration of antennas on PCB [5]. Integrating the antennas in the eWLB package improves the antenna performance because of the low permittivity of the mold material, and short distances between active and passive components. However, as the active side of chip faces the PCB in the eWLB package, the electrical function can be influenced by the PCB and solder balls. Solder balls are typically placed under the chip and beyond including in the mold compound area. In addition, due to different coefficients of thermal expansion (CTE) of the chip and the mold compound, mechanical stresses develop that result in increased warpage of the molded package.

To address this issue as well as improve performance and lower cost, an advanced ultra-thin glass panel embedding (GPE) packaging technology was first developed, by Georgia Tech and its industry partners as the next advance in millimeter wave packaging technology [6]. It is proposed as an ideal solution for millimeter-wave applications for many reasons that include: smaller and thinner package size, lower interconnect loss, large panel processing for lower cost and higher board-level reliability. The high temperature stability of glass in large panel manufacturing makes GPE packages a great choice for automotive applications, which require wider and higher temperature and humidity

operation ranges. Unlike the CTE mismatch between chip and the mold compound, the closer CTE matching between glass and chip as well as glass and board provides a huge advantage resulting in reduced warpage and improved board level reliability. Furthermore, the low-loss tangent of glass, a factor of ~2-3× smaller, compared to that of a typical mold compound, makes GPE an ideal candidate for RF and mm-wave modules [7]. The tailorability of the CTE of glass panels and compliant board level interconnections enable glass to have better board-level reliability as well. Lastly, the development of through glass vias (TGVs) enables the potential for 3D integration of active and passive components in the ultra-thin GPE packages with shorter interconnection lengths.

### 1.4 Research Objectives

The objectives of the proposed research are to model, design and demonstrate ultra-thin and high-performance Glass Panel Embedded (GPE) packages for mmWave applications with lower interconnect loss and higher board-level reliability. The schematic of the proposed GPE package for mmWave applications is shown in Figure 3.

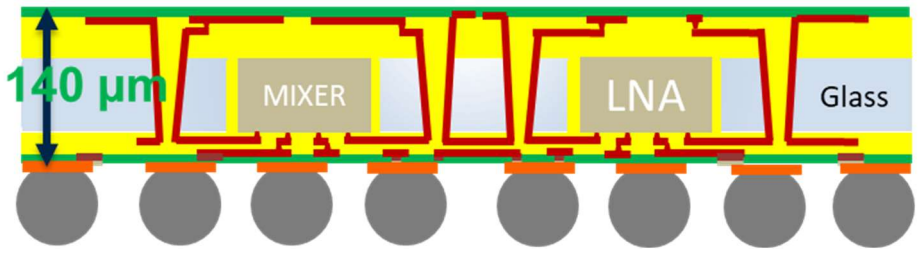



**Figure 3. Schematic of ultra-thin GPE package for mmWave applications**

Two specific goals were defined in this research:

1) Modeling and design of the GPE package with lower interconnect loss and higher electrical performance which include low transmission line loss, low system insertion loss and low TPV loss enabled by miniaturized 3D GPE architecture
2) Fabrication and demonstration of the GPE package with high precision RDL, low warpage, minimized package thickness and high electrical performance.

Table 1 summarizes the detailed parameters associated with the research objectives of this dissertation beyond the prior-art (Wafer-level Fan-out Package).

**Table 1. Research objective beyond prior art.**

| Parameter | | | | Objectives | Prior-Art |
|---|---|---|---|---|---|
| Modeling & design | Miniaturization | | | <150 μm thickness | >450 μm thickness |
| | Performance | T-line loss | | < 0.2 dB/mm | 0.30 dB/mm |
| | | System Insertion loss | | 0.3-0.5 dB | 0.65 dB |
| | | TPV loss | | 0.12 dB | 0.2-0.5 dB |
| Fabrication & Demonstration | Fabrication | | Process tolerance | <20 um dia. microvia | <50 um dia. microvia |
| | | | warpage | < 100 μm warpage on 2 inch panel | >500 μm warpage on 6 inch wafer |
| | Demonstration | | Thickness | <150 μm | >450 μm |
| | | | Electrical Performance | Noise Figure <3dB | Noise Figure >3.4dB |

## 1.5 Technical Challenges and Research Tasks

To achieve these goals, the following research challenges are identified in 1) modeling and design, and 2) fabrication and demonstration, as shown in the schematic cross-section of Figure 4 and summarized in Table 2.

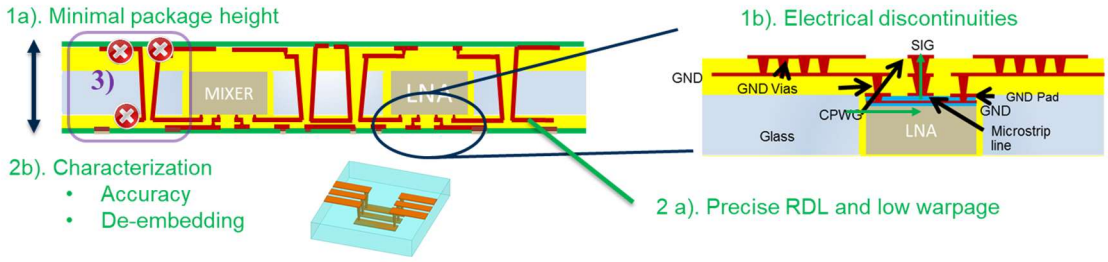



**Figure 4. Schematic cross-section with modeling and design challenges labeled as 1a) and 1b), and fabrication and demonstration challenges labeled as 2a) and 2b).**

**Table 2. Technical challenges and research tasks.**

| | | | Challenges | Tasks |
|---|---|---|---|---|
| 1 a) | Modeling & design: | Miniaturization | • Minimal package height | • Design of package architecture for minimum package thickness |
| 1b) | | Performance | • Electrical discontinuities in die-to-package interconnection | • Modeling and design of embedded chip interconnections with minimum loss |
| 2 a) | Fabrication & Demonstration | Fabrication | • Warpage<br>• Process control of RDL | • Fabrication of GPE package with high-precision & low warpage RDL processes |
| 2 b) | | Demonstration | • Miniaturization<br>  • Ultra-thin glass handling<br>• Performance<br>  • High frequency characterization | • Demonstration of GPE package with minimum pkg thickness<br>• Characterization of noise figure of GPE package |

In modeling and design, one key challenge is to achieve minimal package height. The other challenge in modeling and design of GPE package with high electrical performance is the electrical discontinuities in die-to-package interconnections. As the high-frequency voltage or current signals propagate the end of redistribution layer (RDL) of the chip and are about

to transit through microvias to the package, they see an impedance discontinuity from the junction between RDL and microvias, as shown in Figure 5. Such an impedance discontinuity generates reflections, resulting in time-domain signal degeneration. Therefore, the electrical discontinuity is identified as one major technical challenge in modeling and design of the GPE package.

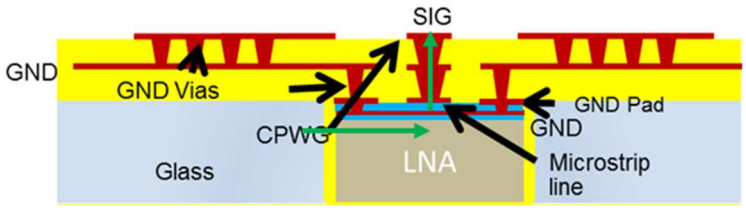



**Figure 5. Impedance discontinuity in die-to-package interconnection.**

In the fabrication of GPE packages, warpage and precision process control of RDL are the two main challenges. In the demonstration of GPE packages with ultra-thin glass panels, handling is critical for miniaturization, the accurate high-frequency characterization and de-embedding are the key challenges for the demonstration of high performance GPE packages.

To address the above challenges, two main research tasks are proposed as summarized in Table 2. Task 1a) is to design package architecture for minimum package thickness. Details of different package architectures are introduced, later in this dissertation. Task 1b) is to model and design embedded chip interconnections with minimum loss. This task contains several sub-tasks including modeling of transmission lines on GPE packages; design and modeling of interconnections; and modeling of package loss in ultra-thin GPE packages. Task 2a) is to fabricate GPE packages with high-precision process control and low warpage.

Task 2b) is to demonstrate GPE packages with minimum package thickness and low system loss & low noise figure.

Many advanced technologies are also studied to address the research challenges to demonstrate GPE packages for mmWave applications. These include:

- Materials: glass as the substrate material with suitable CTE (made feasible owing to the tailorablity of glass CTE, between 3.8 to 9 ppm/$^{o}$K) to reduce the mismatch with chips and superior dimensional stability; ultra-thin and low-loss dielectrics with loss tangent below 0.001.

- Processes: precise glass cavity formation; double carrier process for low warpage; precise microvia drilling for low loss interconnects.

- Mechanical performance: warpage less than 80 μm over a 2 inch glass package; die-shift less than 2 μm.

- Electrical performance: Package insertion loss of less than 0.5 dB.

- Cost: large panel processing for potential lower cost.

# CHAPTER 2. LITERATURE SURVEY

Compared to the traditional flip-chip and wire-bond packages, fan-out wafer level package (FO-WLP) is a great solution for mm-wave applications due to its size, cost, performance and reliability. A major trend in fan-out packaging is the move to large panel formats, so-called fan-out panel level packaging (FO-PLP) to increase productivity and further reduce the cost. This chapter starts with the prior-art on modeling and design of ultra-thin packages for mm-wave applications, followed by the fabrication and demonstration of ultra-thin packages.

## 2.1 Modeling and design of ultra-thin packages for mm-wave applications

### *2.1.1 Advanced Package architecture design*

#### 2.1.1.1 Fan-out Wafer-level Package

Fan-out wafer level packages (FO-WLP) are poised to disrupt the entire semiconductor industry due to their size, cost, performance and reliability benefits compared to traditional flip-chip and wire bond packages. Although they were initially designed to extend package I/O counts beyond fan-in Wafer Level Packages (WLP), the scope of FO-WLP technology has expanded significantly in recent years to include multi-component SiP modules, as well as high I/O logic and memory integration. The driving factors for the implementation of FO-WLP technology are the associated low packaging and test costs, excellent electrical and thermal performance, improved reliability compared to WLP, and the potential for heterogeneous integration.

A typical fan-out wafer-level package architecture design is shown in Figure 6. The fan-out wafer-level package architecture consists of 1) two or more dielectrics, 2) conductors deposited on to 3) Al or Cu pads on the BEOL of devices, 4) embedded IC that is embedded in a 5) molding compound, and 6) Pb-free solder balls to attach the FO-WLP package to the board. By embedding the chip inside the substrate package, the interconnections between the chip and package or board are very short, and thus improves the electrical performance.

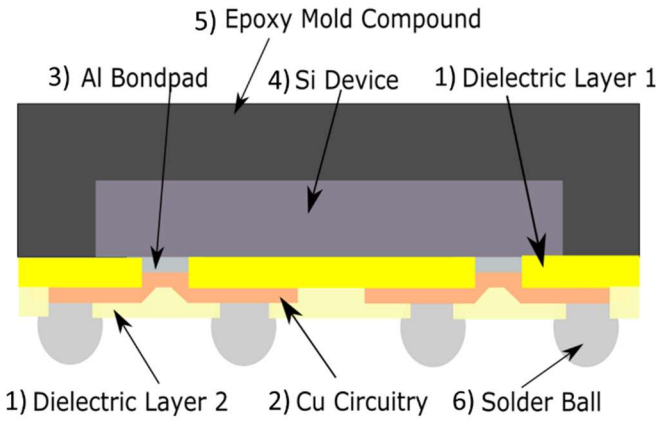



**Figure 6. Package architecture design of fan-out wafer-level package.**

Wafer-level fan-out packages have many advantages that include:

- Shortest interconnection length and hence highest electrical speed

  In Figure 7, two packages are considered. Figure 7 a) is a flip-chip package with a flipped chip assembled on an organic substrate, and chip-to-substrate interconnections including under fill (UF) and solder bumps. Figure 7 b) is a fan-out wafer-level package. The signal lengths and hence the signal delays between these are very different. The fan-out wafer level package in Figure 7b) has much

improved electrical performance than in Figure 7a) because of the reduced signal path lengths.

- No substrate required from the package foundry which means reduced processing and cost
- No assembly for the first – level chip assembly to the substrates
- Ultra-thin package as a result of a) embedding of ultra-thin ICs and b) absence of substrate and solder joints for assembly.
- Improved board-level reliability by virtue of higher CTE and lower modulus of the molding compound.
- Allows larger ICs to be packaged compared to WLP.
- Smaller foot print than flip-chip or wire-bonded packages.


**Figure 7. Signal loss contributions in a) Flip-chip package vs b) Fan-out wafer-level package**

2.1.1.2 Fan-Out Panel-level Packages

A major trend in fan-out packaging is the move to large panel formats, so-called panel level packaging (FO-PLP) to increase productivity and further reduce cost. The economies of

scale up panel-based processing may reduce FO-WLP cost from 20-40 %, up to 2-4×, depending on the package and panel sizes, and the number of dies per package.

FO-PLP technologies can be broadly classified into 1) laminate embedded solutions, such as Imbera's Integrated Module Board (IMB) [12], AT&S's Embedded Components Packaging (ECP) [13], and ASE's advanced – Embedded Assembly Solution Integration (a-EASI) [14]; 2) panel fan-out solutions, including Amkor/J-Devices Wide Strip Panel Fan-out Package (WFOP) [15], PTI's panel-scale molded fan-out, and 3) chip-last FO-PLP, such as ASE's coreless embedded trace approach. Panel sizes up to 24'' × 18''/610 mm × 457 mm have been demonstrated by applying current laminate or PWB infrastructure, or new hybrid process lines [16, 17].

There are many different approaches to panel-level packaging. But the general idea is to embed the ICs within the laminate substrate, board, or molded encapsulant first, and then use the substrate build-up technologies to create the RDL. **Error! Reference source not found.** shows the schematic cross-section of a FO-PLP package. Though the cross-section of PLP is similar to FO-WLP, the process is very different. The FO-WLP process uses the wafer back-end fabrication materials, processes, and tools that are the same as in WLP, whereas in PLP, the process is similar to building up laminate substrate processes. Thus FO-WLP has finer line capability, even though limited by the molding compounds than within the build-up circuitry with PLP. One significant advantage of PLP over FO-WLP is its lower cost, because it does not use high-end fab-like materials, processes, or tools, and has higher productivity due to the increased size.

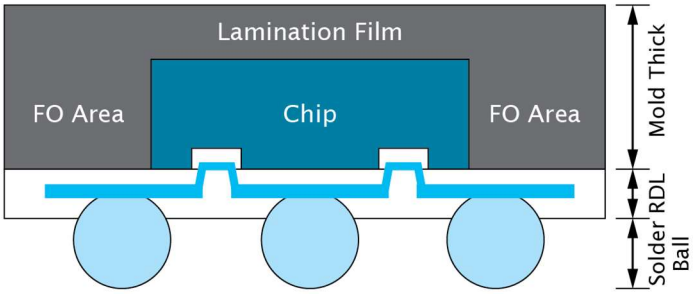



**Figure 8. Package architecture design of fan-out panel-level package.**

Compared to the traditional flip-chip and wire-bond packages, FO-WLP and FO-PLP provide great solutions for mm-wave applications due to its size, cost, performance and reliability. However, there is a continuing need to improve I/O density, high-frequency performance, yield & cost and board-level reliability beyond current FO-WLP and FO-PLP approaches. This need can be comprehensively addressed by using glass as the fan-out substrate.

### *2.1.2 Modeling and design of parasitic elements*

FO-WLP provides improved electrical performance because of shorter interconnection length than the traditional wire-bonded or flip-chip packages. The package schematics and 3D electrical modeling of flip-chi BGA package and eWLB were shown in Figure 9 [10]. These package designs are carried out with functional devices to investigate package level performance in real applications. In 3D simulation works, a few critical pins are selected and studied, such as clock, VDD as well Data pins.

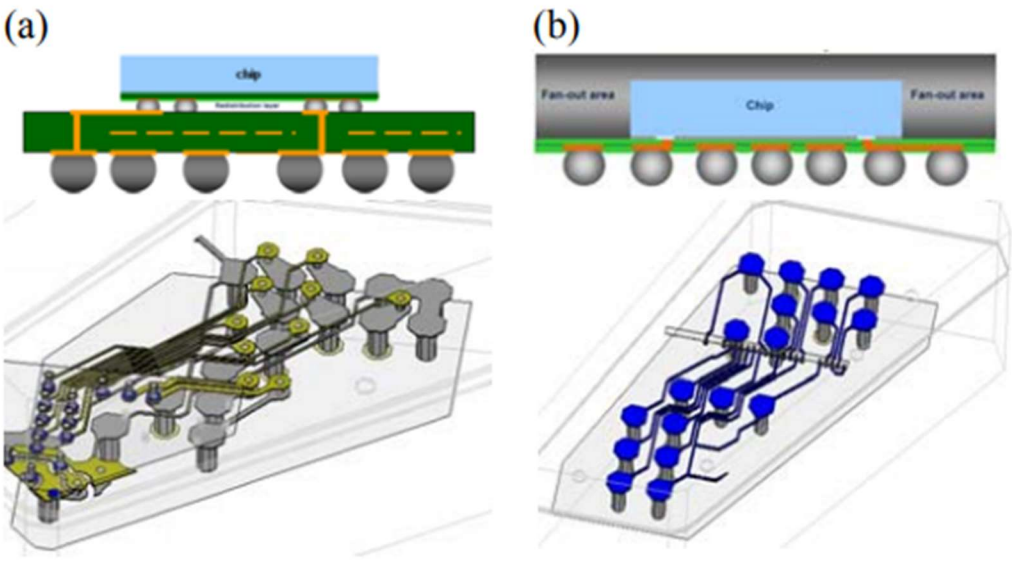



**Figure 9. Package schematics and electrical modeling of a) flip-chip BGA and b) eWLB for electrical simulation (STATS ChipPAC)**

In comparison to a flip-chip BGA package, FO-WLP has less parasitic values of R, L, and C, resulting in improved signal transmission performance. As shown in Figure 10, the eWLB, which is a typical type of FO-WLP, has 68 percent less resistance, 66 percent less inductance, and 39 percent less capacitance compared to traditional flip-chip BGA [10]. It is mainly due to shorter interconnection in eWLB. For flip-chi BGA package, there are flip-chip solder bump and substrate interconnections all contribute signal delay. eWLB has shorter interconnection with RDL process thus, it has improved electrical performance than flip-chip BGA package.

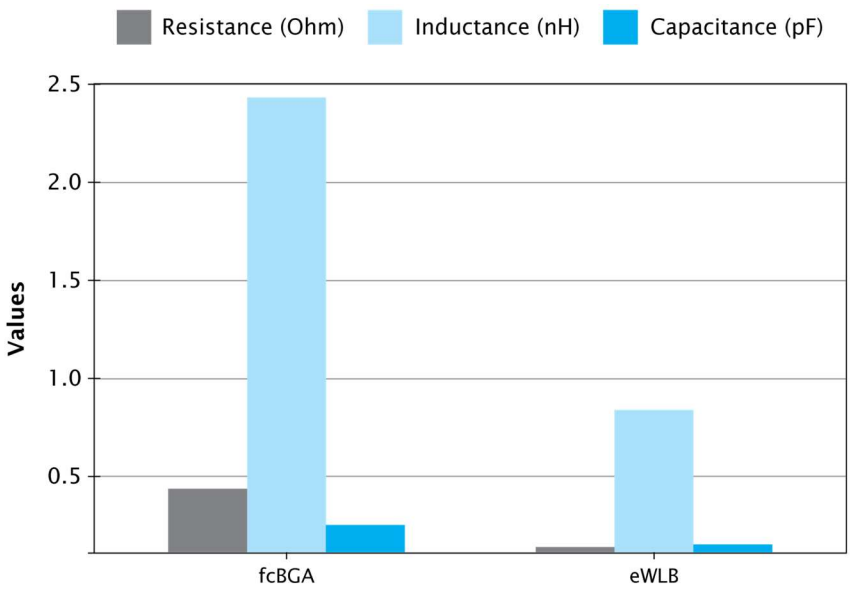
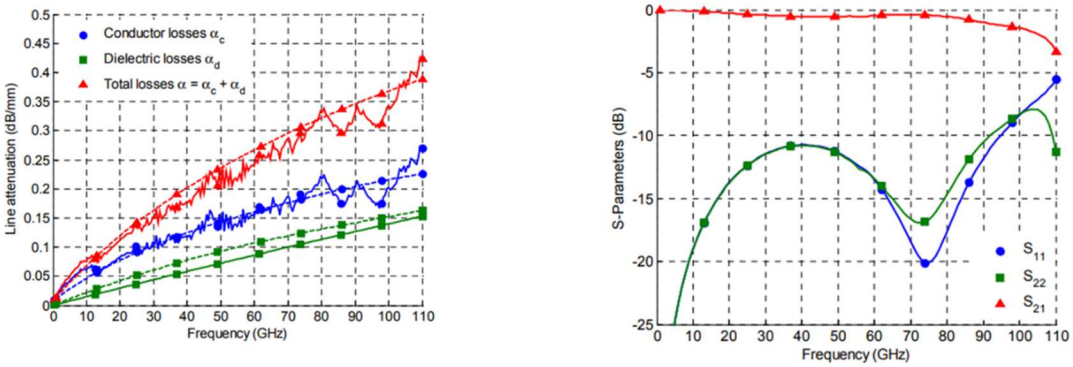



**Figure 10. Electrical parameters: resistance (R), inductance (L), and capacitance (C) of traditional flip-chip BGA package (fcBGA) vs. FO-WLP @ 1 GHz (STATS ChipPAC)**

### *2.1.3 Modeling and design of transmission line loss and insertion loss*

Figure 11a) illustrates the measured and simulated frequency dependent contributions of the conductor and dielectric losses to the attenuation of a 50 Ω CPW in eWLB. The attenuation at lower frequencies is mainly due to losses in conductors (90% at 1 GHz). However, as the frequency increases, the contribution of losses in dielectrics increases (already 30% at 10 GHz and 40% at 110 GHz). The eWLB package can achieve transmission-line loss as low as 0.32 dB/mm [20] at 77GHz.

By an appropriate printed circuit board (PCB) and RDL design, the impact of the transition-related parasitics can be minimized and compensated without resorting to external matching. Figure 11 illustrates simulated return and insertion loss of an optimized chip-package-board transition in an eWLB. An insertion loss as low as −0.65 dB and a return loss below −16 dB at 77 GHz are observed [21].



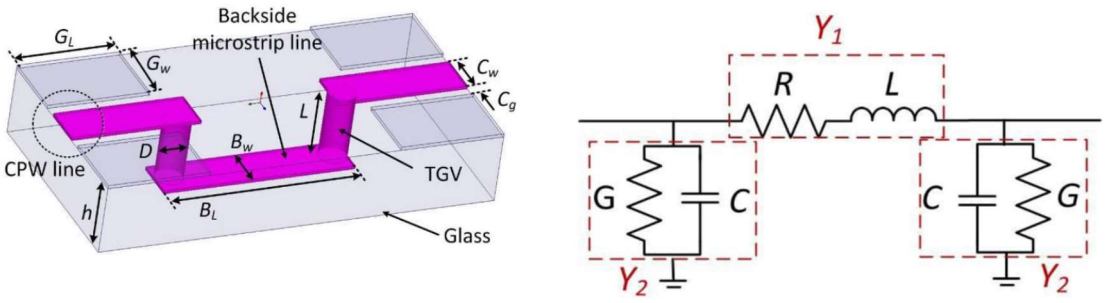

(a) eWLB transmission-line loss (b) eWLB insertion loss and return loss

**Figure 11. eWLB electrical performance: (a) transmission-line loss 0.32 dB/mm @ 77 GHz, (b) insertion loss -0.65 dB and return loss below -16 dB @ 77 GHz**

### *2.1.4 Modelling and design of TPVs*

Through-package-vias (TPVs) are key components in a package for mm-Wave applications. The coupling noise and cross-talk are both effected by TPVs.

Kim [24] from University of Florida modeled TPVs in glass substrates shown in Figure 12 (a), as an equivalent $\pi$-circuit model in Figure 12 (b), and the lumped element parameters (*RLGC*) were extracted from 3D EM simulations. It was pointed out that the TPV with a diameter of 90 μm and a height of 500 μm, buried in a glass substrate with $\varepsilon_r = 7.9$ and $\tan\delta = 0.008$, had a resistance of 2.2 Ω, an inductance of 0.3 nH, a conductance of 0.01 S, and a capacitance of 1.8 pF at 1 GHz.




(a) (b)

**Figure 12. (a) Perspective view of the dual-via chain structure, and (b) equivalent π-circuit model.**

Hwang [25] from KAIST of South Korea studied the TPV-to-TPV noise coupling to a 2.4 GHz low-noise amplifier (LNA) in Radio-frequency (RF) glass interposers, as shown in Figure 13 (a). A modified noise figure equation was proposed to include the TPV-to-TPV noise. From the time and frequency domain simulations, it was confirmed that the LNA output waveform was distorted by the coupling noise, and with a 10 mV TPV-to-TPV noise coupling to LAN, the noise figure was degraded by 13 dB at 2 GHz, as shown in Figure 13 (b). In addition, Hwang [26] studied the TPV noise coupling for 2.5-D and 3D glass interposers. Equivalent circuits were proposed and validated by 3D EM simulations in frequency domain. Finally, two methods were proposed to reduce TPV coupling noise: 1) increasing signal-to-signal TPV pitch, as shown in Figure 13 (c), and 2) inserting ground TPVs around signal TPVs, as shown in Figure 13 (d).

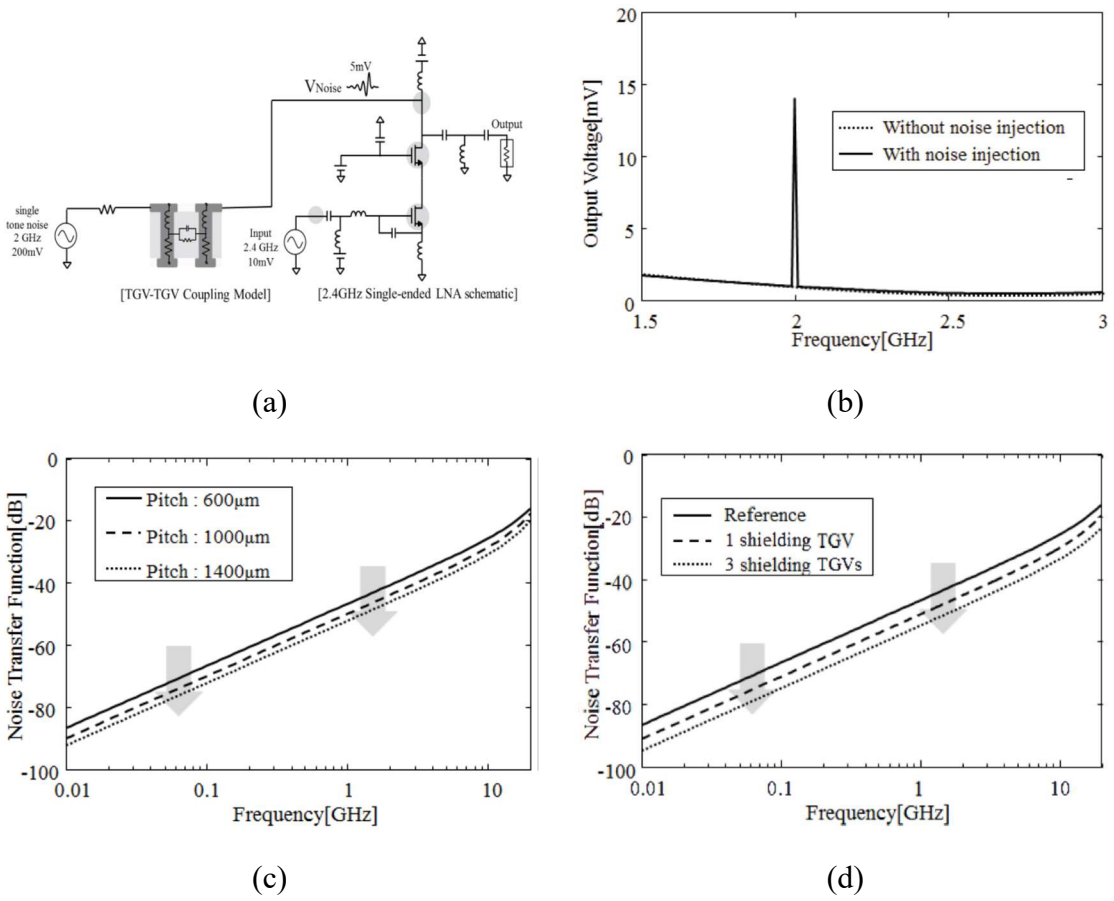



**Figure 13. (a) Schematic view of noise coupling through TPVs to LNA, (b) simulated LNA output waveform with and without TPV coupling noise, (c) functions of noise coupling with different signal via pitch, and (d) functions of noise coupling with different numbers of inserted ground vias.**

## 2.2 Fabrication and demonstration of ultra-thin packages for mm-wave applications

Mechanically, FO-WLP differs from wire-bonded or flip-chip packages because they do not require first level assembly (FLA) or chip assembly such as wire-bonds or solder bumps. By eliminating the chip-level assembly, FO-WLP minimizes the interconnect stress and avoids inter-layer dielectric (ILD) cracking and delamination issues. In addition, FO-WLP improves board-level reliability by virtue of higher coefficient of thermal expansion (CTE) and lower modulus of the molding compound than Si devices. Further, FO-WLP packages are thinner and smaller than those of equivalent flip-chip and wire-bond packages due to the finer design ground rules enabled by fab-like processes.

### *2.2.1 Process flow for advanced package fabrication*

A typical FO-WLP process starts with singulated devices from the wafer that are picked and placed on an adhesive tape, on a 200 mm or 300 mm carrier wafer. The most common carrier wafers are silicon and glass. The reconfigured wafer is then molded with an epoxy mold compound. The molding extends the surface size of the chip thus allowing more bumps to be placed, as shown in Figure 14. The carrier is then removed, and the molded or reconstituted wafer is flipped over, followed by depositing the redistribution layers (RDL). Finally, the solder balls are placed over the RDL wiring layers using a stencil, the wafer then is fluxed and reflowed. After reflow and flux clean, the parts are ground to the final thickness, laser marked, and then singulated into the final packages. Such a process results in thinnest form factor with short signal path lengths and high electrical performance.

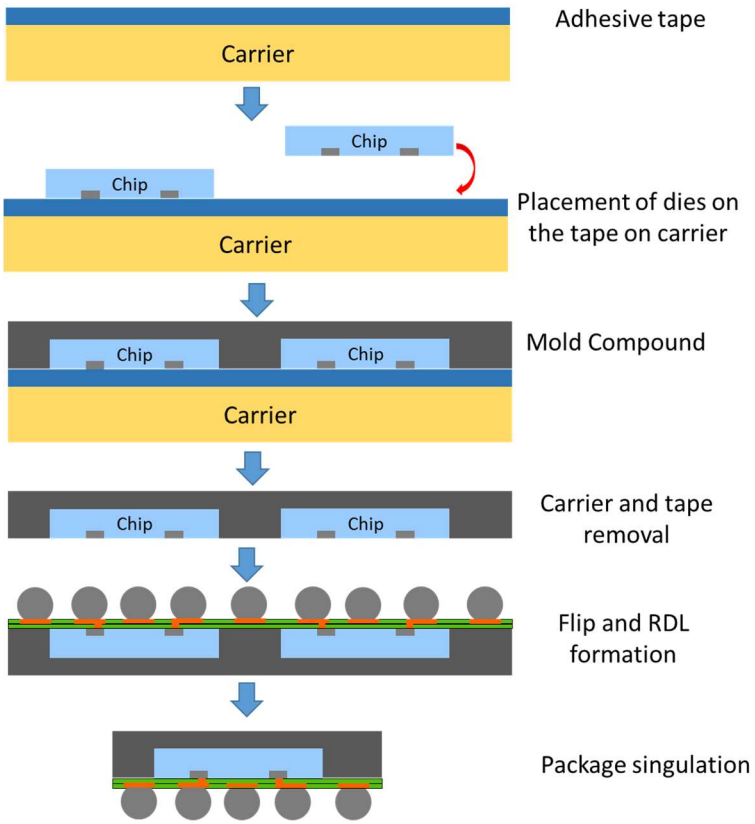



**Figure 14. Fan-Out Wafer Level Package (FO-WLP) packaging process flow**

### *2.2.2 Advanced solutions for warpage reduction*

Warpage is a key challenge in fabrication and demonstration of ultra-thin packages due to the CTE mismatch between the chip and the substrate. One way to reduce the warpage is to optimize the fabrication process flow and conditions, as shown in Figure 15a) [27]. Another way is to apply warpage adjustment tool after thermal debonding, as shown in Figure 15b) [28].

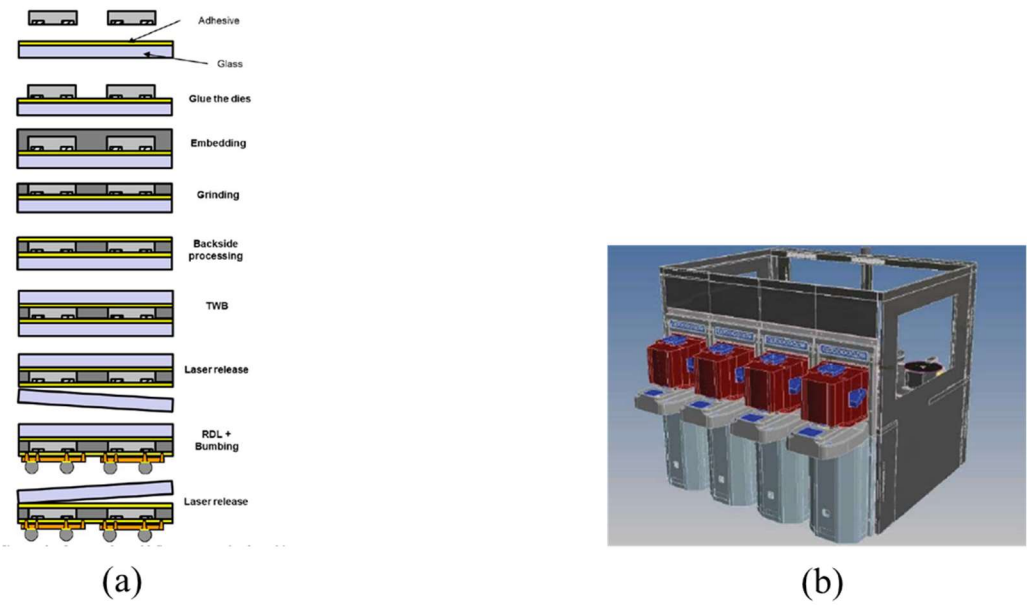



**Figure 15. Advanced warpage reduction solutions: a) Improved process flow, b) Applied warpage adjustment tool after thermal debonding.**

### *2.2.3 Demonstration of ultra-thin Panel-level Fan-out Package*

As introduced in previous sub-section, fan-out panel-level package is a great solution for mm-Wave applications and can further reduce the cost compared with wafer-level fan-out package. The Embedded Silicon Fan-out (eSiFO) Package, one example of fan-out panel-level package, was demonstrated with the package thickness to be as low as 200 μm [29], as shown in Figure 16.

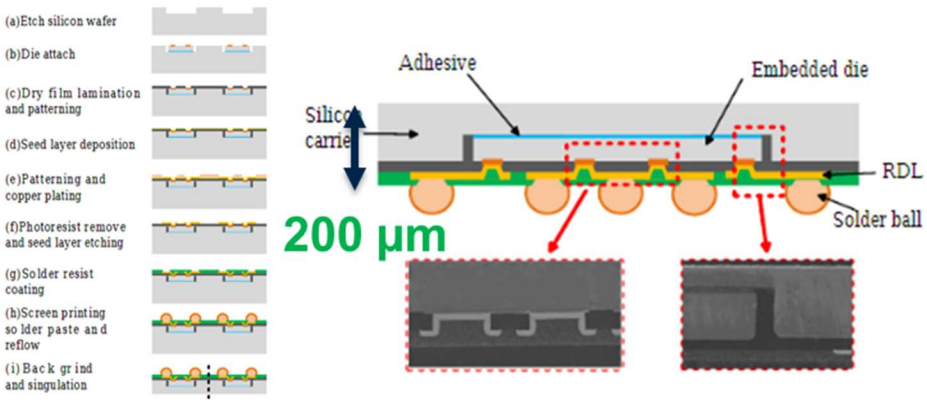



**Figure 16. Demonstration of ultra-thin Panel-level Fan-out Package with package thickness as low as 200 µm.**

However, such an ultra-thin panel-level fan-out package requires the process of etching silicon wafer of the chip and back grinding after embedding the chip. These processes can be expensive and increase the cost. By applying the ultra-thin GPE approach, there is no need for back grinding.

### *2.2.4 Fabrication and demonstration of RADAR modules*

Two examples of advanced RADAR modules are shown in **Error! Reference source not found.Error! Reference source not found.**, Freescale's redistributed chip packaging (RCP) for TMTT 2012 RADAR module [18] and Infineon's embedded wafer level ball grid array packaging (eWLB) for RFIC 2012 RADAR module [19]. These advanced RADAR modules can achieve improved electrical performance at high frequency enabled by the advanced packing architecture with short interconnection length. The eWLB package can achieve transmission-line loss as low as 0.32 dB/mm [20], insertion loss as low as -0.65 dB and return loss below -16 dB at 77 GHz [21] without external matching networks.

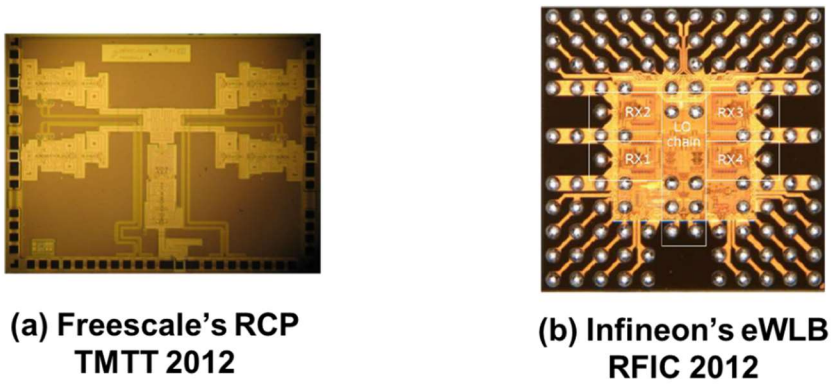



**Figure 17. Two examples of advanced RADAR modules: (a) Freescale's redistributed chip packaging (RCP), (b) Infineon's embedded wafer level ball (eWLB) grid array packaging**

However, the size of Freescale's RCP and Infineon's eWLB packages for RADAR module is less than 6 mm × 6 mm, with the thickness over 300 μm. This can be improved by ultra-thin GPE packages with larger package size and minimized package height as low as 140 μm, and with potential to enable even lower losses.

# CHAPTER 3. MODELING AND DESIGN OF ULTRA-THIN GPE PACKAGES FOR MM-WAVE APPLICATIONS

## 3.1 Design of package architecture for minimum thickness

### *3.1.1 Mechanical Modeling*

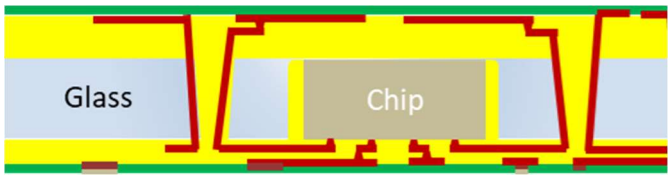



**Figure 18. Anatomy of an ultra-thin GPE package**

The anatomy of an ultra-thin GPE package is shown in Figure 18. It consists: (1) two or more dielectrics, (2) embedded IC that is embedded in (3) a glass cavity, and (4) mircrovias connecting the Al or Cu pads on the embedded chips to the package, and (5) through glass vias. The mechanical modeling and electrical modeling are based on this package stack up.

The mechanical modeling mainly focused on the warpage analysis of the package. To achieve the minimum warpage, a symmetric stack-up is usually needed. However, for ultra-thin GPE packages, the top dielectric filling the glass cavities can be different from the bottom dielectric concerning the reliability of the package. In this case, a stack-up with one glass layer in the middle, and different dielectrics with different thickness on each side was modeled to achieve minimum warpage. The properties of the two dielectrics employed in this study and glass are shown below in Table 3**Error! Reference source not found.**.

**Table 3. Properties of dielectrics and glass in ultra-thin GPE packages**

| | Unit | Dielectric A | Glass | Dielectric B |
|---|---|---|---|---|
| CTE | ppm | 15 | 3.8 | 30 |
| Modules | GPa | 15 | 77 | 7.5 |
| Thickness | μm | 40 | 100 | 20 x n |

To compensate 40 μm thick dielectric A, dielectric B with different thickness were modeled. As shown in Figure 19, 20 μm dielectric B has the minimum warpage with 40 μm thick dielectric A.

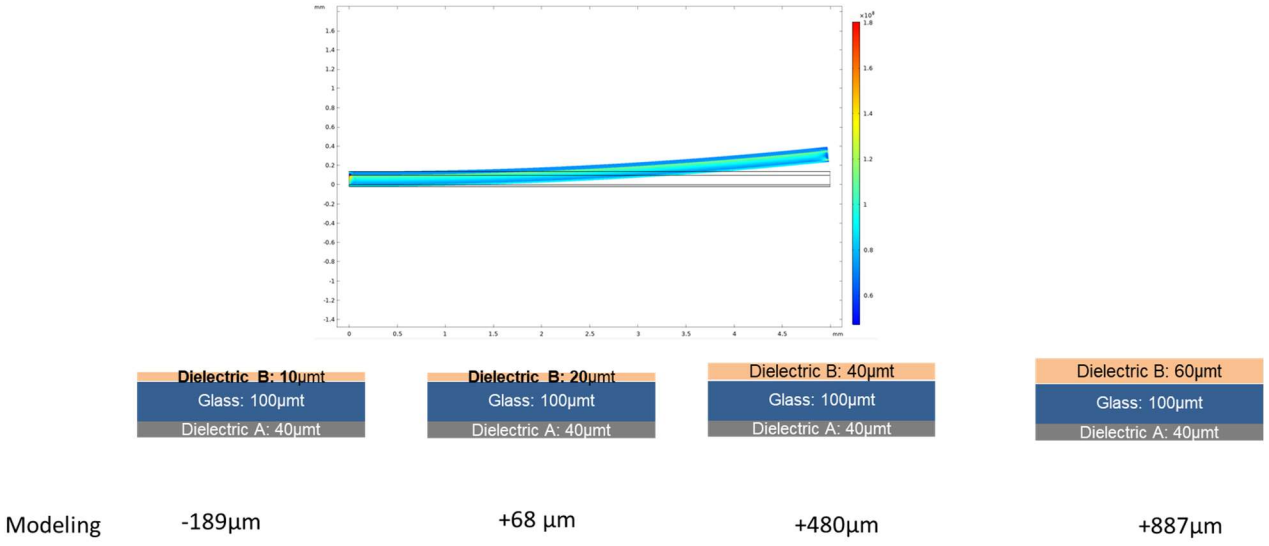



**Figure 19. Modeling results of warpage in ultra-thin GPE packages**

### *3.1.2 Design of GPE package*

To make it clear, the GPE package in this section refers to a package with thickness as low as 200 μm, while the ultra-thin GPE package refers to a package with thickness as low as 140 μm. The different architecture designs of GPE packages and ultra-thin GPE packages will be introduced in this section.

#### 3.1.2.1 Design of GPE package with through cavity

The package architecture design of a GPE package with through cavity is shown in Figure 20. The total thickness is less than 220 µm, including a 50 µm thick glass carrier, a 70 µm thick glass cavity panel, 75 µm thick test chips embedded in the glass cavity, the bonding dry film and the double-side RDL polymers.


**Figure 20. Package architecture design of GPE package with through cavity**

3.1.2.2 Design of GPE package w/ blind cavity

The package architecture design of a GPE package with blind cavity is shown in Figure 21. The total thickness is less than 240 µm, including a 200 µm glass substrate with 100 µm thick blind glass cavity, 100 µm thick test chips embedded in the glass cavity, and the double-side RDL polymers.


**Figure 21. Package architecture design of GPE package with blind cavity**

*3.1.3 Design of ultra-thin GPE package without glass carrier*

The package architecture design of an ultra-thin GPE package without glass carrier is shown in Figure 21. The total thickness is less than 140 µm, including a 100 µm thick glass

cavity, 100 μm thick test chips embedded in the glass cavity, and the double-side RDL polymers.

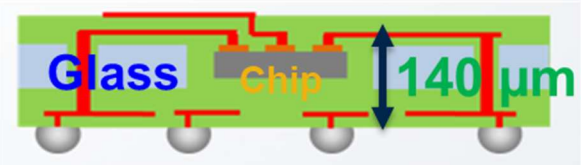



**Figure 22. Package architecture design of ultra-thin GPE package without glass carrier**

Compared with the GPE package, the ultra-thin GPE package can provide a) smallest z-height, b) easier TPV formation, c) lower loss enabled by shorter signal path, d) explosion of the backside of the chip, and it provides advantages such as possible direct chip cooling from the back side. The ultra-thin package required precise RDL control and minimum warpage, which will be introduced in Chapter 4.

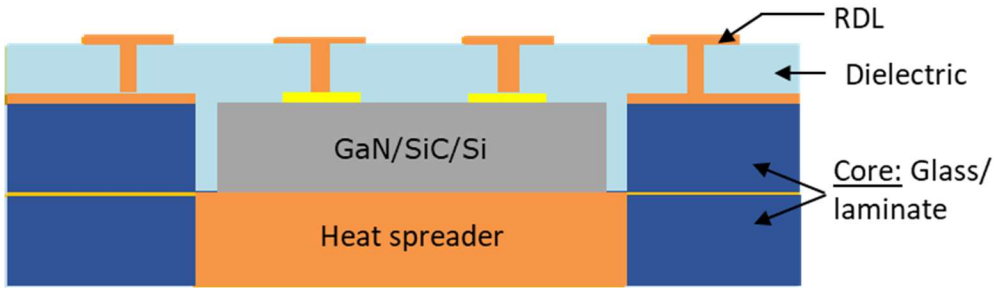



**Figure 23. Package architecture design of direct cooling for ultra-thin GPE package [31]**

## 3.2 Modeling and design of embedded chip interconnection with minimum loss

### *3.2.1 Modelling of transmission lines on GPE*

As shown in Figure 24, four different types of transmission lines: microstrip line, strip line, CPW, and CPWG on ultra-thin GPE packages were simulated to analyse the insertion

loss at high frequencies (0-150GHz) for mm-Wave applications. The dielectric thickness was set to be 20 μm, and the Cu height was set to be 10 μm. Though microstrip line is easier to fabricate and is less influenced by the fabrication variation, it suffers the increased insertion loss into the mm-wave frequency range, making the circuit technology less efficient for use at frequencies of 30 GHz and beyond. Based on the simulated results shown in Table 4, microstrip line and strip line have much larger insertion loss than the CPW and CPWG at higher frequencies. The insertion loss of CPWG is similar to that of CPW at high frequency. Since CPWG can share the same ground with the microstrip line, and has less radiation loss than CPW, it is selected for the signal transmission for GPE package.

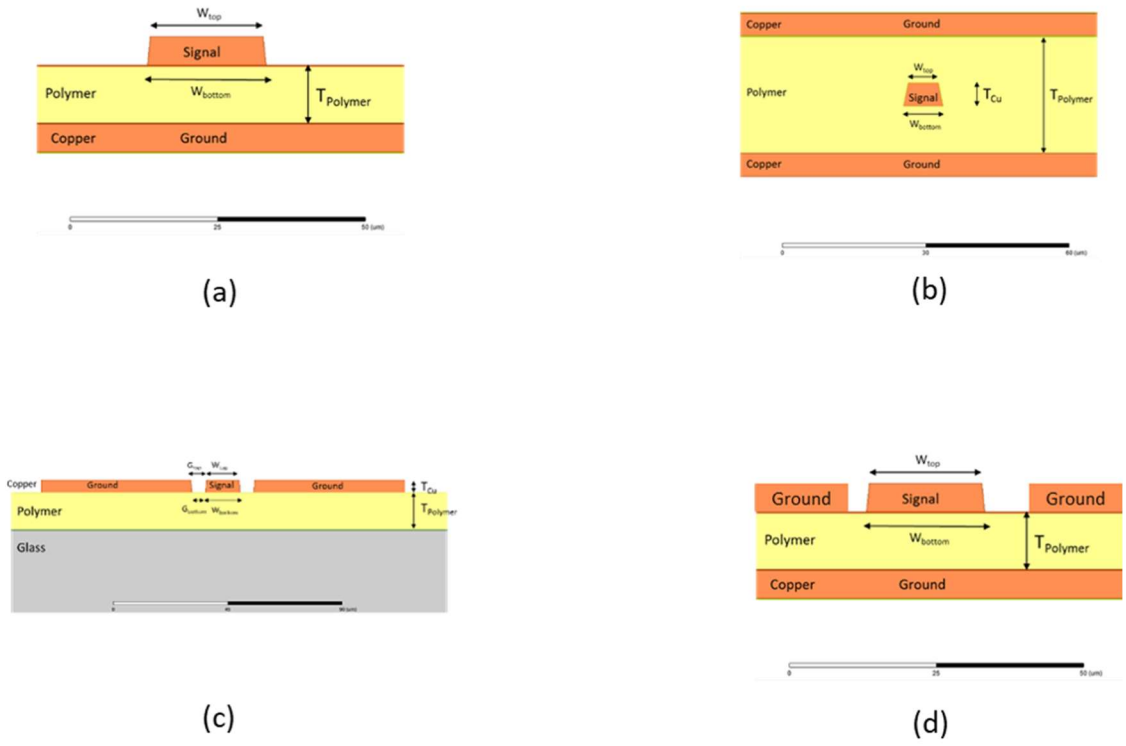



**Figure 24: Different types of transmission lines on ultra-thin GPE packages: (a) microstrip line, (b) strip line, and (c) CPW, and (d) CPWG.**

**Table 4: Insertion loss of different types of transmission lines at different frequencies**

| T-line | Insertion Loss dB/mm @ 10 GHz | Insertion Loss dB/mm @ 77 GHz | Insertion Loss dB/mm @ 140 GHz |
|---|---|---|---|
| Microstrip line | 0.095 | 0.286 | 0.586 |
| Strip line | 0.093 | 0.253 | 0.465 |
| CPW | 0.087 | 0.176 | 0.231 |
| CPWG | 0.088 | 0.177 | 0.233 |

Different types of low loss dielectrics were also modelled for CPWG structure. The dielectric thickness was set to be 20 µm, and the Cu height was set to be 10 µm. For each different material, the Cu width of the CPW was calculated based on the dielectric constant and loss tangent of each dielectric. Figure 25 shows the modelling result of CPWG line on GPE package using ABF GY11. The detailed properties of different materials and simulated results were shown in Table 5. BCB resin series with a loss tangent as low as 0.0008 has the minimum insertion loss as low as 0.14 dB/mm at 77GHz among all the selected dielectrics.

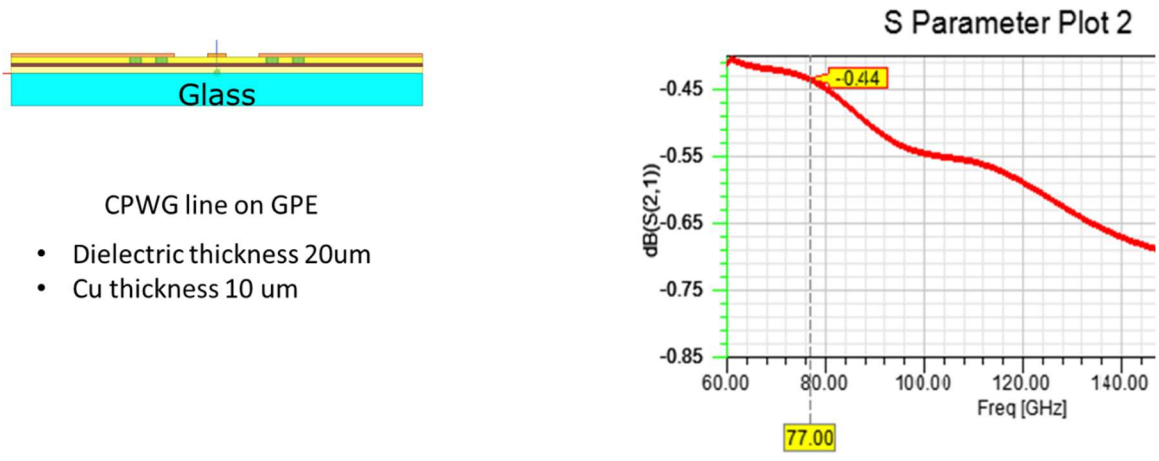



**Figure 25: Modelling of CPWG lines on ultra-thin GPE packages**

**Table 5. Simulated results of CPWG line insertion loss at 77 GHz with different dielectrics on ultra-thin GPE packages**

| Dielectrics | Dk | Df (loss tangent) | Insertion Loss dB/mm |
|---|---|---|---|
| ABF GY11 | 3.2 | 0.004 | 0.177 @ 77GHz |
| BCB 14-P005 | 2.59 | 0.006 | 0.178 @ 77GHz |
| BCB CYCLOTENE 4000 Resin Series | 2.65 | 0.0008 | 0.140 @ 77GHz |
| Epoxy Dry Film | 3.1 | 0.02 | 0.313 @ 77GHz |

### *3.2.2 Design and Modelling of interconnections*

As shown in Figure 266, a model of ultra-thin GPE package was established. A silicon chip embedded in the glass cavity, on top of the chip a microstrip line was created, with a pad on top of the surface to be connected to RDL layers on the packages. A CPWG transmission-line on the glass package was created connecting the chip signals through microvias. The loss of the microstrip lines on the chip and the CPWG lines on the glass package was first simulated separately following which the loss of the whole structure was simulated. By de-embedding the loss of the t-lines on the chip and package, the loss of the interconnections through microvias can be evaluated.

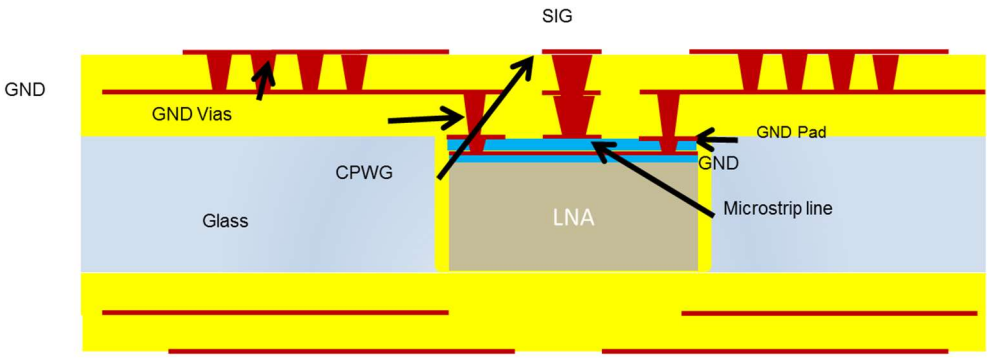


**Figure 26: Anatomy of ultra-thin GPE package interconnects**

As shown in Table 6, when the size of the pad is closer to the size of the via, the interconnection loss is lower. This means high microvia position accuracy can help reduce the size of pads on top of the die I/Os for the signal transmission, which in turn will reduce the parasitic effect and provide low loss interconnections.

**Table 6: Interconnection loss @ 77 GHz with different pad size on ultra-thin GPE packages**

| Pad and via size | Pad dia. 30 um<br>Via dia. 20 um  | Pad dia. 60 um<br>Via dia. 20 um  |
|---|---|---|
| Loss @ 77GHz | 0.12 dB | 0.16 dB |

### *3.2.3 Modelling of TPVs in Ultra-thin GPE Packages*

As shown in Figure 277, the signal transition, impedance discontinuity, and the crosstalk of TPVs in ultra-thin GPE packages were studied for improved signal integrity.

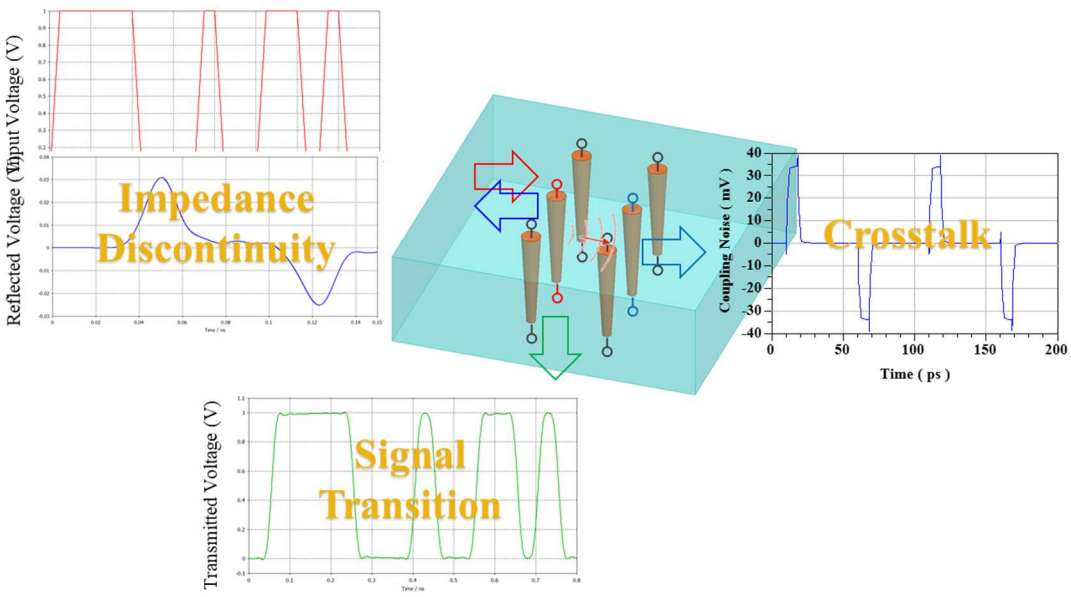
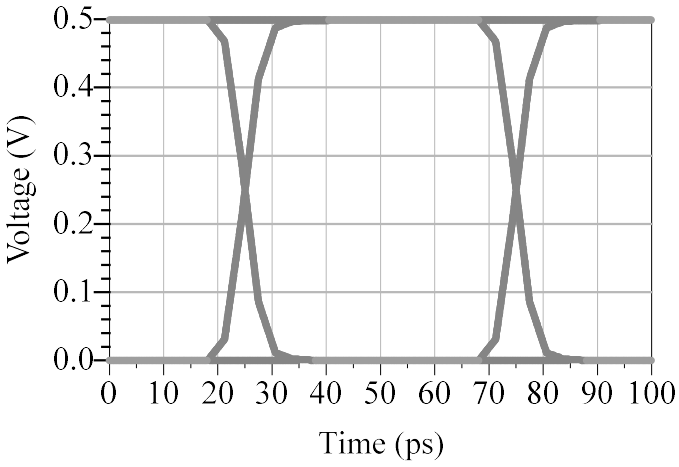


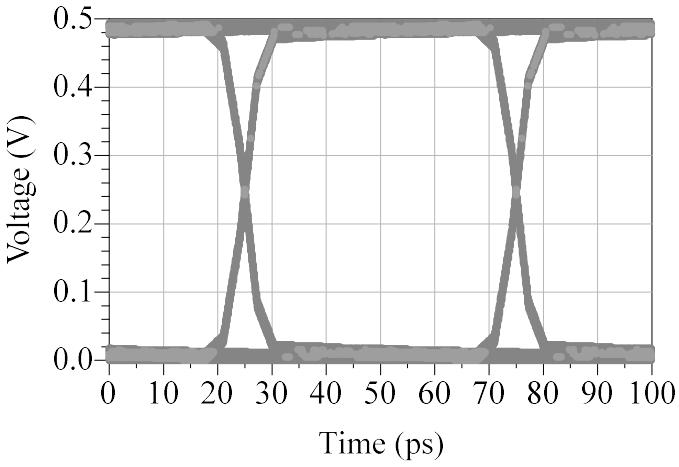

**Figure 27. Modeling and design of TPVs for improved SI**

3.2.3.1 Signal transition

Based on the frequency-domain *S*-parameters, eye-diagram simulations were conducted to analyze the time-domain degeneration for signals transiting through TPVs. The time-domain pseudo-random bit sequence had a length of $2^{10}$-1, with a 5-ps rise-and-fall time. The bit rate was set to 20 Gbps, and the source impedance was set to 50 Ω. The high-level voltage was 1 V, while the low-level voltage was 0 V. Each bit was sent at the top of TPVs and recorded at the bottom of TPVs to generate eye diagrams. The simulated eye diagrams of 30-μm TPVs in 150-μm glass interposers are shown in **Error! Reference source not found.** (a), and those of 30-μm TSVs in 150-μm silicon interposers are shown in **Error! Reference source not found.** (b) for comparison. It can be seen from Figure 28 that both eye diagrams are widely open, because the test structures include only the TPVs or TSVs. Compared with TSVs in silicon, TPVs in glass have better eye opening, primarily due to the low substrate loss in glass.




(a)




(b)

**Figure 28. Simulated eye diagrams of (a) TPVs in glass interposers and (b) TSVs in silicon interposers at a bit rate of 20 Gbps.**

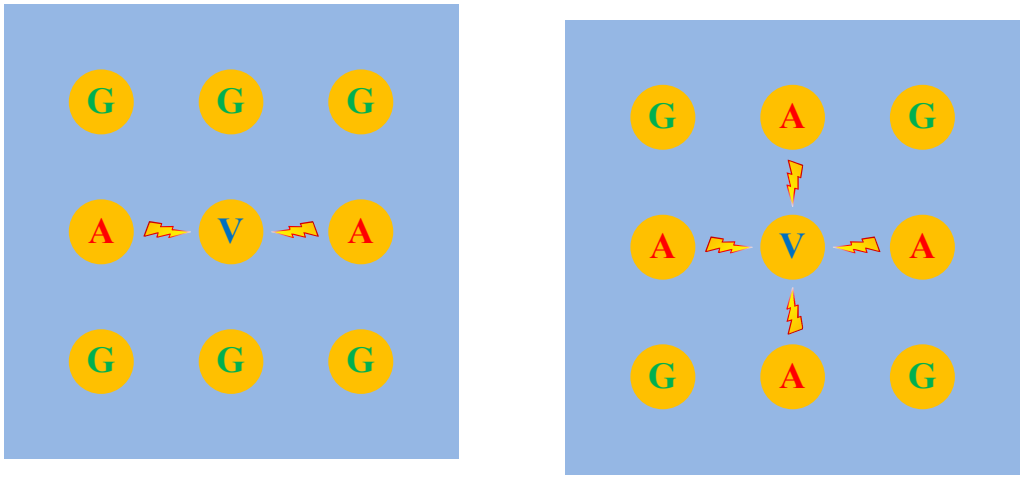
3.2.3.2 Impedance discontinuity

One of the challenges for TPV design is the impedance discontinuity: when the incident signal travelling along RDLs reaches the electrical interface between RDL and TPVs, it encounters a different impedance of TPVs, resulting in reflection which degenerates the signal transition through TPVs and might be the source of electromagnetic interference

(EMI). The time-domain reflectometry (TDR) responses indicate that there is an inductive discontinuity due to TPVs. To reduce the inductive discontinuity, inserting multiple ground TPVs around a signal TPV can bring down the characteristic impedance, leading to less inductive discontinuity [30].

#### 3.2.3.3 Crosstalk

In practice, TPVs in glass interposers are placed in close proximity to each other to enable high interconnection density. Thus, when a TPV is active in sending signals, called an aggressor, an inactive TPV, called a victim, might be affected by crosstalk noise coupled from the aggressor. Two worst cases were studies, as shown in Figure 299.



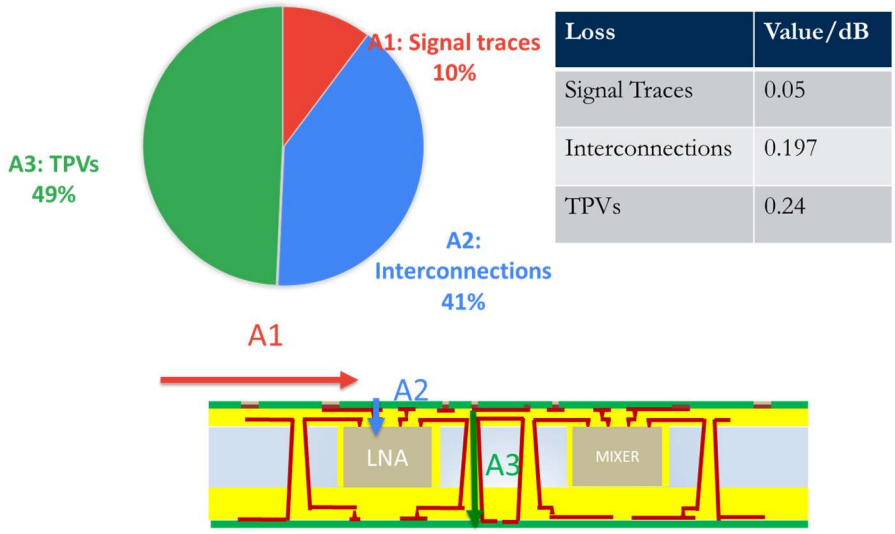

(a) (b)

**Figure 29. Top view of two worst-case via configurations: (a) two aggressors and one victim (A2V1), and (b) four aggressors and one victim (A4V1).**

The simulation results show that doubling the number of aggressor TPVs to one victim TPV increases the crosstalk amplitude by more than twofold. Hence, when designing TPVs in glass interposers, it is preferred to keep the number of aggressor TPVs as low as possible.

### 3.2.3.4 Modelling of Package Loss for Ultra-thin GPE Packages

The whole package loss of the ultra-thin GPE package including the loss of the signal traces, interconnections and TPVs were first simulated separately and then summarized. When the transmission-line length is minimized, the simulated results show that the whole package loss of the ultra-thin GPE package can be less than 0.5 dB, shown in Figure 3030.




| Loss | Value/dB |
|---|---|
| Signal Traces | 0.05 |
| Interconnections | 0.197 |
| TPVs | 0.24 |

**Figure 30. Modelling of Package Loss for Ultra-thin GPE Packages**

# CHAPTER 4. FABRICATION AND DEMONSTRATION OF ULTRA-THIN GPE PACKAGE FOR MM-WAVE APPLICATIONS

## 4.1 Fabrication of GPE package with high precision process control and low warpage

In this section, glass panel embedding (GPE) packages with different types of glass cavities and dies were first demonstrated. Then the ultra-thin GPE package was proposed and demonstrated with even smaller package thickness. The details of the fabrication will be described the sections below.

### *4.1.1 High precision process control*

#### 4.1.1.1 Process test vehicle design

The purpose of the process test vehicle is to test the precision of each fabrication process step including TPV metallization, microvia drilling, RDL fabrication, die assembly and BGA balling. Dummy test dies with daisy chain structures were fabricated by ASE Group on 300 mm wafers, as shown in Figure 31 (a), to emulate logic dies. The die is designed at a standard size of 10 mm x 10 mm to emulate high-end Application Processors (AP), with 1856 signal I/Os at 40/80 μm pitch in 4 peripheral staggered rows and 3592 power I/Os at 150 μm pitch in a central area array, for a total of 5448 I/Os as shown in Figure 311 (b) and (c).

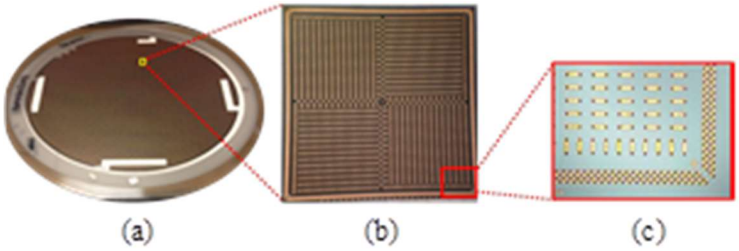



**Figure 31. Daisy chain test dies fabricated by ASE (a) on 300 mm wafer, (b) one single die from the 300 mm wafer, and (c) snap shot of die corner.**

A four metal layer fully-integrated glass package was designed to connect all 5448 chip I/O bumps to the substrate, as shown in Figure 322. Among the chip I/O bumps, 176 of those were connected through chip-level interconnections, and TPVs, and board-level interconnections to the board. The top view of the glass package layout design is shown in Figure 33(a), which includes the layout of four metal layers, top and bottom solder resist, as well as the location of BVs and TPVs. This fully-integrated glass substrate design coupon, which measured 15 mm x 15 mm, was then panelized to fit in a 150 mm x 150 mm glass panel. Due to the exposure range of the projection aligner used (provided by Ushio Inc.), which is a 100 mm circle, the coupon is laid out in a 5 x 3 array with 0.5 mm dicing street, and exposed twice to achieve 30 coupons in a panel, as shown in Figure 333 (b).

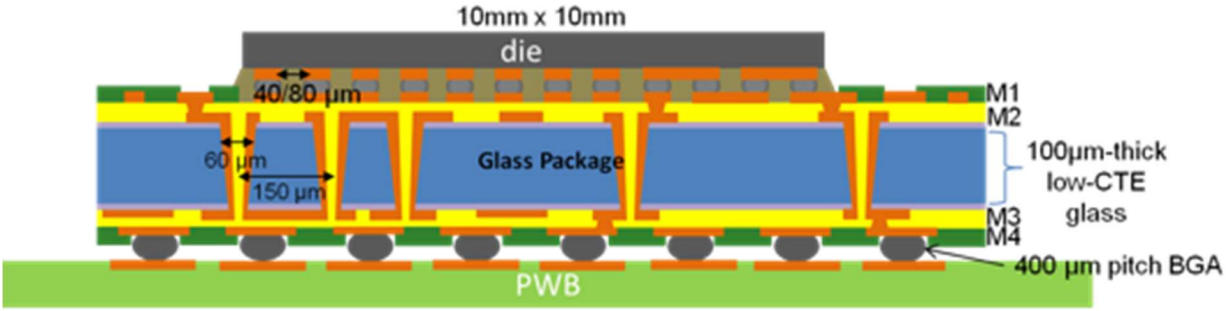



**Figure 32. Cross section of the process test vehicle with 40/80µm minimum I/O pitch.**

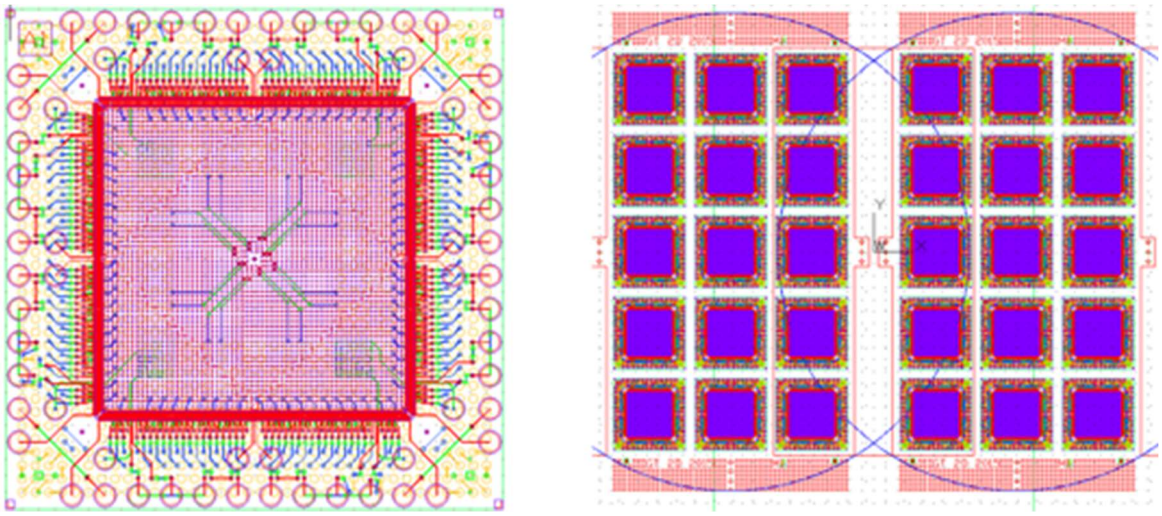
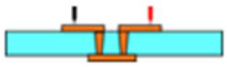
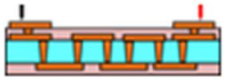
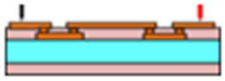
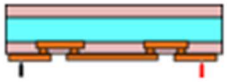
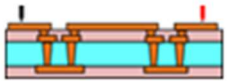
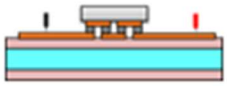
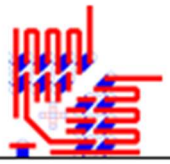
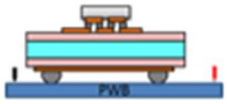
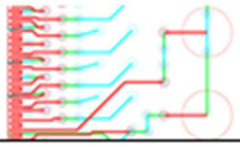
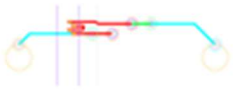


**Figure 33. Top view of substrate layout design of (a) single fully-integrated glass package coupon at the size of 15mm x 15mm x 0.1 mm, and (b) 30 coupons in total on a 150mm x 150mm glass panel.**

Multi-level test structures were designed to evaluate the yield at each fabrication process step, as shown in Table 77. Nine types of test structures were designed, including TPV daisy chains, BV daisy chains, chip-level interconnection daisy chains, and other multi-layer test structures. The first five types are substrate-level test structures to be tested during each phase of substrate fabrication for yield evaluation. The last five types require the assembly of the dummy die. Only type 7 require board level assembly, as the primary focus of present study is on the reliability of die-to-substrate interconnections. Type 8 and type 9 are the most extensive test structures, with the only difference being the inclusion of bottom blind via & M4 for type 9 test structures.

**Table 7. Multi-level Test Structures for Yield Evaluation.**

| Type | Schematic | Layers | Description | Top View Layout |
|---|---|---|---|---|
| 1 |  | M2-M3 | TPV chains |  |
| 2 |  | M1-M3 | |  |
| 3 |  | M1-M2 | BVs |  |
| 4 |  | M3-M4 | |  |
| 5 |  | M1-M3 | Substrate |  |
| 6 |  | Die-M1 | Chip-level DCs |  |
| 7 |  | M4-PWB | Board-level DCs |  |
| 8 |  | Die-M3 | CLI + Substrate |  |
| 9 |  | Die-M4 | CLI + Substrate |  |

Relatively relaxed design rules based on previously achieved results were applied to optimize the yield to focus the study of process variability in fabrication and assembly. The

design rules are summarized in Table 88. The minimum line and space is set at 20/20 µm to facilitate yield, but has limited routing capability in the 40/80 µm pitch signal I/O area. As a result, fine line escape routing is not included in the test structures.

**Table 8. Summary of Design Rules.**

| **Design Rules** | | | |
|---|---|---|---|
| Glass thickness | 100 µm | Min. L/S | 20/20 µm |
| Glass body size | 15 mm x 15 mm | BV diameter | 80 µm |
| Logic die size | 10 mm x 10 mm | BV pitch | Min. 150 µm |
| Chip-level pitch | 40/80 µm | TPV diameter | 60 µm |
| BGA pitch | 400 µm | TPV pitch | Min. 150 µm |

4.1.1.2 Fabrication

The fully-integrated glass packages were fabricated on a 150 mm x 150 mm low-CTE glass panel that is 100 µm thick. The illustrated fabrication process flow and stack-up specifications of the fully-integrated glass package are shown in Figure 344 and Table 99 respectively.

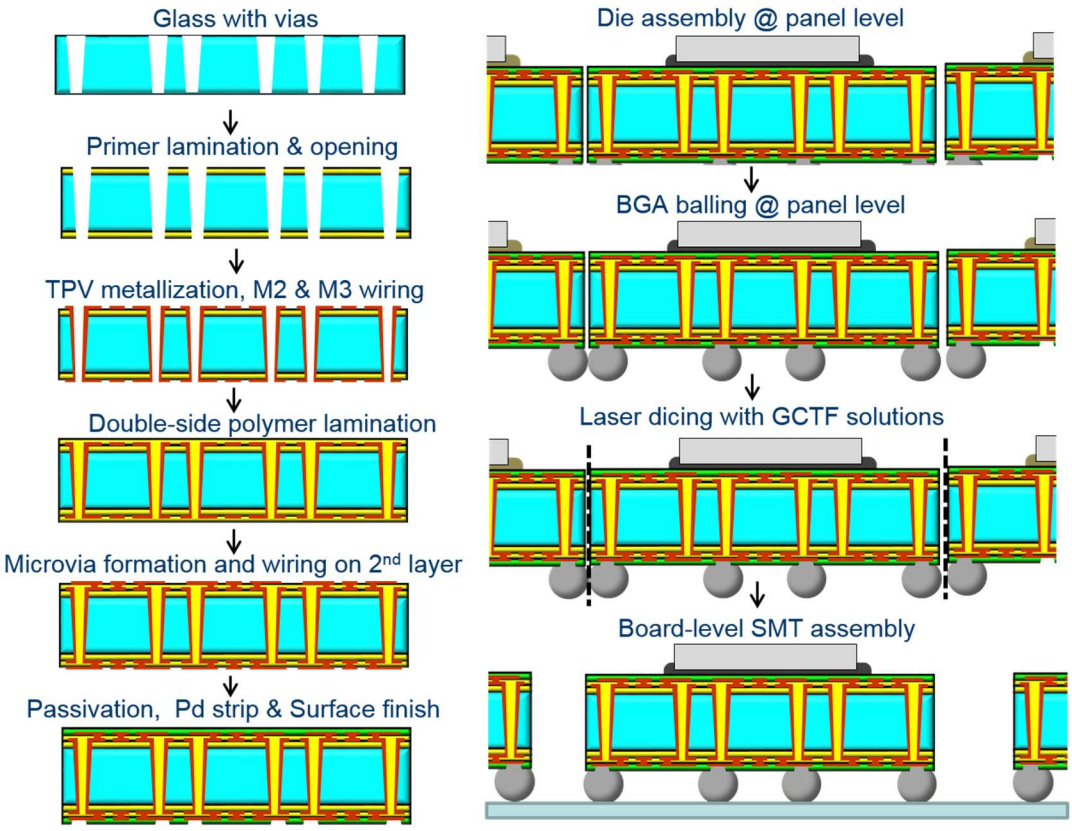



**Figure 34. Process TV fabrication process flow.**

**Table 9. Process TV Stack-up Specification**

| | Thickness (μm) | Material | Resource |
|---|---|---|---|
| Solder Resist | 10~15 | SR-FA | Hitachi Chemical |
| 1st layer polymer | 5 | ABF GX-92P | Ajinomoto |
| 2nd layer polymer | 15 | ABF GX-92 | Ajinomoto |
| Glass | 100 | EN-A1 | Asahi Glass Company |

In this test vehicle, TPVs at 150 μm pitch were achieved by a via-first process, which utilized via formation on bare glass by Asahi Glass Company, followed by primer

lamination and opening with a high-throughput plasma etching method. The primer material used is a dry-film dielectric provided by Ajinomoto Inc., called ABF, which can be processed at a low temperature of 180°C. In addition, the surface of ABF is suitable for electro-less plating of copper seed layer, which allowed the use of semi-additive process (SAP). SAP utilizes electrolytic plating of lithographically defined patterns on the copper seed layer to pattern multi-layer copper traces at a minimum of 20/20 μm line and space. Finer pitch could be achieved by optimization of copper seed layer etching, but was not pursued in this design to maximize yield. To create four metal layers, two SAP steps were performed. The first SAP step was responsible for patterning M2 and M3, as well as the conformal plating of TPVs. ABF was used again as the dielectric layer between the first-level metallization and second-level metallization. The blind microvias were formed by laser drilling of ABF and electro-less plating of both the ABF surface and the via sidewalls. The second SAP step completed the patterning of M1 and M4, as well as the conformal plating of blind vias on either sides of the glass panel.

The passivation layer used is a dry-film based material provided by Hitachi Chemical. Similar to ABF, this material can be processed at a low temperature of 180°C. The pad connections to the die cannot be solder mask defined as the pitch requirement exceeded the capability of the dry-film material. Instead, a bump-on-trace routing structure was used as shown in Figure 355. Two main fabrication challenges from previous fabrication cycles can be improved by applying such fan-in fan-out bump-on-trace routing structure. One is the surface finish bridging caused by extraneous plating of nickel on the Cu trace with small features, and the other one is the difficulty to have small, individual passivation openings to support the fine-pitch signal I/Os. The bump-on-trace routing structure brings

coarser Cu trace width and spacing design rules, and thus reduces the surface finish bridging risk. Further, it accommodates a slit solder resist opening, providing better passivation alignment accuracy and avoiding the passivation resolution challenge.

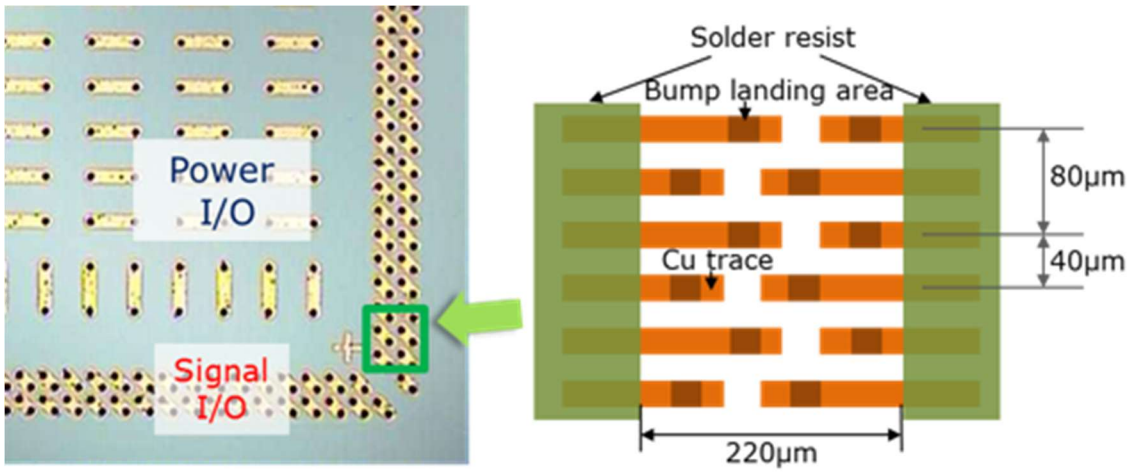



**Figure 35. Bump-on-trace structure for die signal I/Os.**

The bump-on-trace structure does have one additional process requirement: the use of pre-applied underfill materials for chip-level assembly to confine the solder and limit its spread over the exposed trace due to slit opening.

Based on the process flow described above, twelve glass panels and six organic panels as dummy samples were fabricated in three batches. Figure 366 (a) shows the fabricated glass substrate on a 150 mm x 150 mm square glass panel, while Figure 366 (b) shows the cross-section of the glass substrate with Cu traces on four metal layer, TPVs of ~60 µm diameter (Figure 366 (c)), and BVs of ~90 µm diameter (Figure 366 (d)), which enables the signal to travel from M1 to M3 through BVs and TPVs, and back to M1.

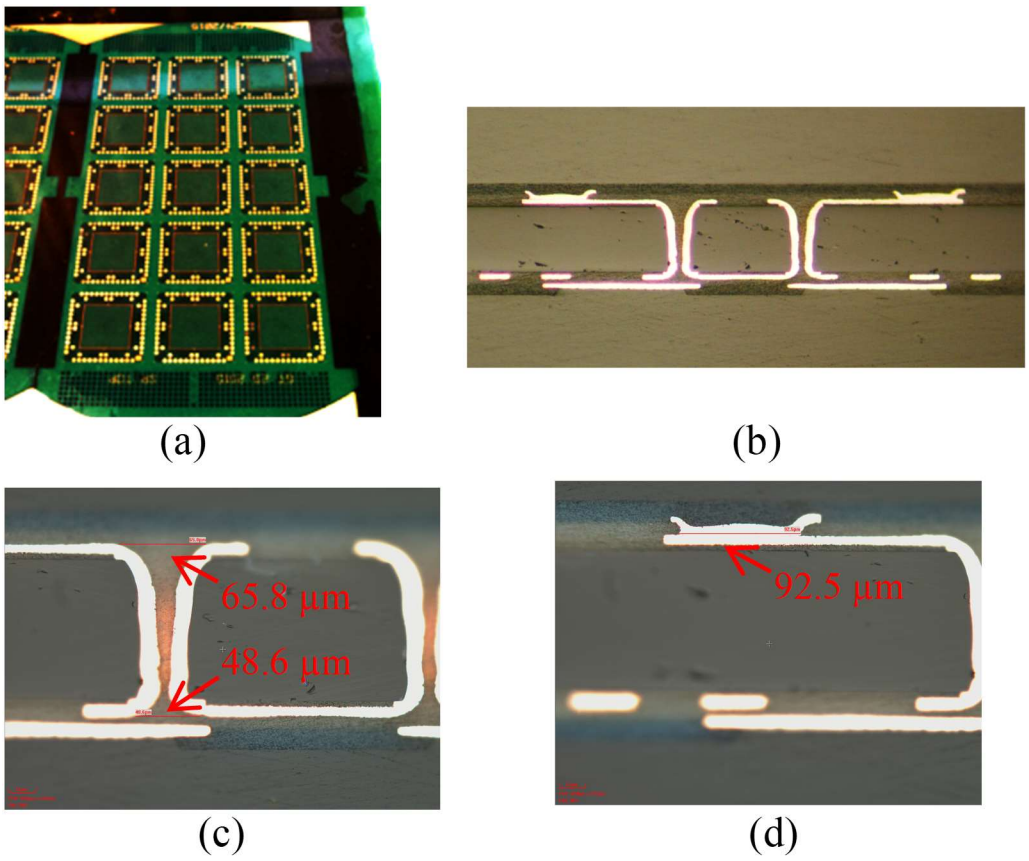


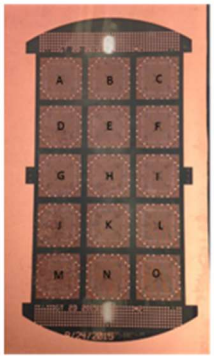

**Figure 36. (a) Fabricated glass substrates on a 150mm x 150 mm square glass panel. (b) Cross-section of the glass substrate at 20x magnification, (c) TPV at 50x magnification, (d) BV at 50x magnification.**

As shown in Figure 344, once surface finish, usually by a wet process such as electroless nickel immersion gold (ENIG) plating, is applied, substrate processing is considered completed.

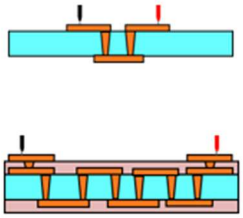
Yield for each fabrication process was evaluated by DC resistance characterization of the multi-level test structures listed in Table 7.7

TPV yield was evaluated on a 75 mm x 150 mm glass half-panel, which consists of 15 coupons in total, as shown in Figure 37 (a). For each coupon, DC resistances of TPV daisy-

chain test structures which connect 264 TPVs in total were measured to calculate the TPV yield of each coupon. As shown in Figure 377 (b), an over 99% TPV yield, was achieved by via-first process with plasma etching primer drilling method.




(a)

| Test Structure | Yield Evaluation | | |
|---|---|---|---|
|  | 100% | 100% | 100% |
| | 100% | 99% | 100% |
| | 100% | 100% | 100% |
| | 99% | 100% | 100% |
| | 100% | 99% | 100% |

(b)

**Figure 37. TPV yield evaluation on (a) a 75mm x 150 mm square glass panel. (b) Test structure and TPV yield results.**

Similarly, the BV yield of 12 coupons was evaluated based on the measurement of DC resistances of BV daisy-chain test structures. The results show that the yield is over 99%. Excellent yield was therefore confirmed for each substrate-level process step. The die assembly, performed at panel level, is shown next.

Die-to-glass panel assembly was achieved by thermo-compression (TC) bonding with the novel, high-speed, chip-to-substrate (C2S) APAMA fully-automated production bonder from Kulicke and Soffa. The glass substrates, diced into 75 mm × 150 mm halves, were first cleaned with isopropanol alcohol, dried with a $N_2$ gun, then baked for one hour at 150°C. Non-conductive paste (NCP) from Namics Corporation with a filler content of 50-65% was then precisely dispensed on each bonding sites to an equivalent volume of 18 mg, in a star pattern. The temperature of the stage onto which the substrates were vacuum-held

was maintained at 70°C throughout the process. Such low stage temperatures are required, given the typical thermal stability on stage of epoxy-based NCPs, to guarantee no evolution in the material's properties for at least the time it takes to fully populate a substrate strip. The tool head temperature, on the die side, was first ramped up to 120°C with an 800 ms dwell time and a maximum ramp rate of 200 K/s, then to the peak temperature of 300°C, maintained for 2 s. A bonding force of 40 N was applied through the whole process. An assembled glass substrate strip, comprising 15 dies bonded with the described TC process, is shown in Figure 388.

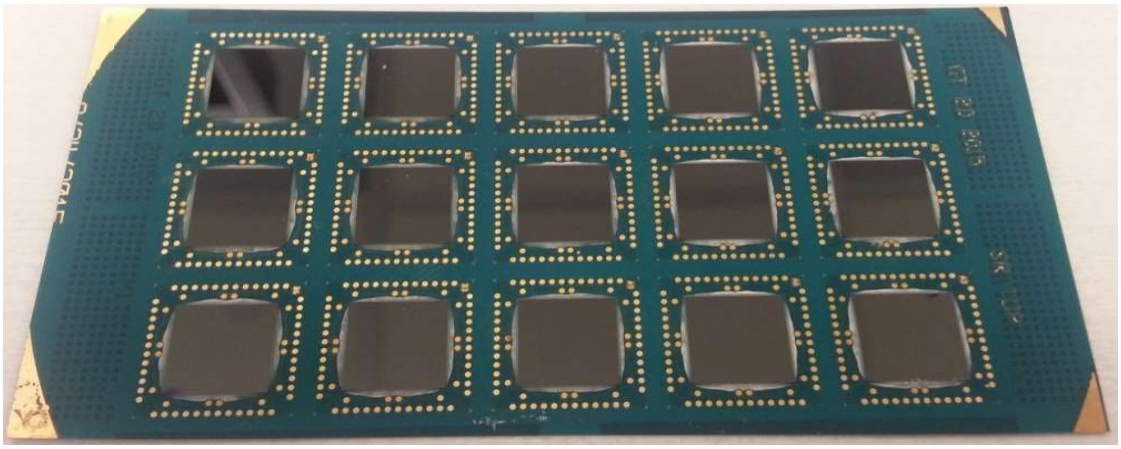


**Figure 38. Glass substrate strip after die assembly by TC-NCP.**

The cross-section of an assembled coupon in Figure 399 shows well-formed bump-on-trace Cu pillar inter-connections, with the typical shape expected from TC-NCP processing. Good alignment and solder collapse were achieved with optimized bonding conditions. No significant filler entrapment could be observed within the solder.

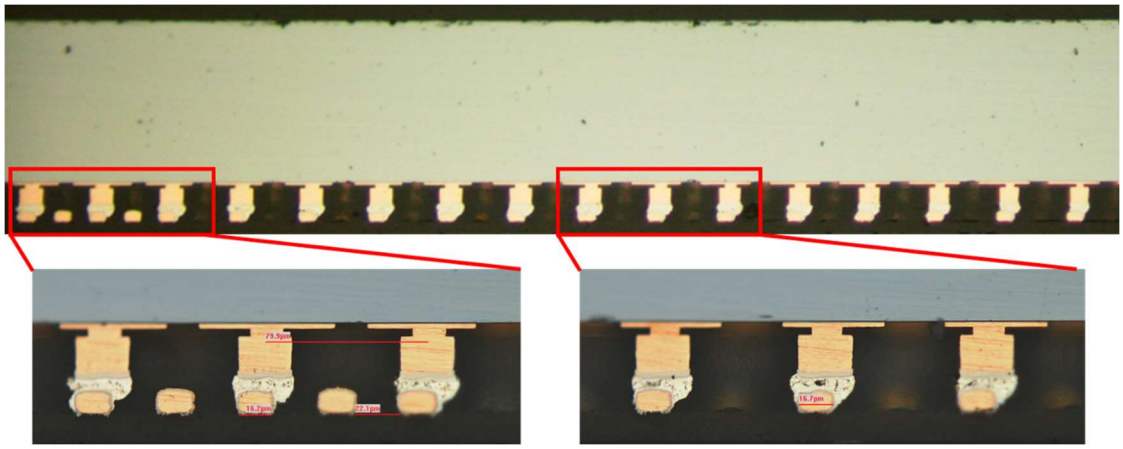


**Figure 39. Cross-section of a singulated glass package.**

Additionally, the assembled strips were found very flat after chip-level assembly, on account of the high modulus (~80 GPa) and glass transition temperature (~550°C) of glass which enabled lower warpage compared to organic substrates of same CTE [7]. Warpage mitigation constitutes one of the key benefits of glass packaging, suggesting potentiality of extending direct SMT assembly of glass BGA packages to the board at body sizes larger than achievable with current packaging technologies, with improved board- and system-level reliability.

Assembly yield was assessed by DC measurements of the chip-to-M1 daisy-chain resistances, including four corner and four inner chains with 20 and 58 bumps, respectively. The results of this evaluation are reported in Table 10 for three fully-integrated coupons with full yield at package level. All but one chain were electrically functional, with little discrepancies in resistance values between coupons, suggesting a high chip-level assembly yield.

**Table 10. Chip-level Assembly Yield Evaluation**

| Coupon | Corner Chain Resistance (Ω) | | | | Inner ChainResistance (Ω) | | | |
|---|---|---|---|---|---|---|---|---|
| 1 | 1.23 | 1.43 | 1.34 | 1.23 | 2.78 | 3.13 | × | 2.85 |
| 2 | 1.20 | 1.54 | 1.80 | 1.36 | 3.17 | 3.42 | 3.69 | 3.27 |
| 3 | 1.45 | 1.45 | 1.40 | 1.51 | 3.40 | 3.35 | 3.61 | 3.56 |

In summary, the fabrication of this process test vehicle demonstrated the high precision process control for each fabrication step.

### *4.1.2 Fabrication and Demonstration of GPE packages*

#### 4.1.2.1 Demonstration of GPE packages with through glass cavities

##### 4.1.2.1.1 Process flow

The process flow for the fabrication of GPE package with through glass cavities is shown in Figure 4040. Glass panels with 70 μm thickness and through-glass cavities were first fabricated with precise cavity location and dimensional accuracy below +5 μm, and then bonded onto a 50 μm thick glass panel carrier using adhesives, but not cured in order to retain tackiness for subsequent die-assembly process. After glass-to-glass bonding, the test dies were assembled into the glass cavities using a high-speed placement tool (Kulicke and Soffa). RDL polymers were then laminated onto both sides of the glass panels, and simultaneously cured to minimize the warpage of the ultra-thin package. A surface planarization (fly-cut) tool by Disco was then used to planarize the surface of the panel and expose the copper microbumps on the die. Fan-out redistribution traces were formed following a standard semi-additive process (SAP).

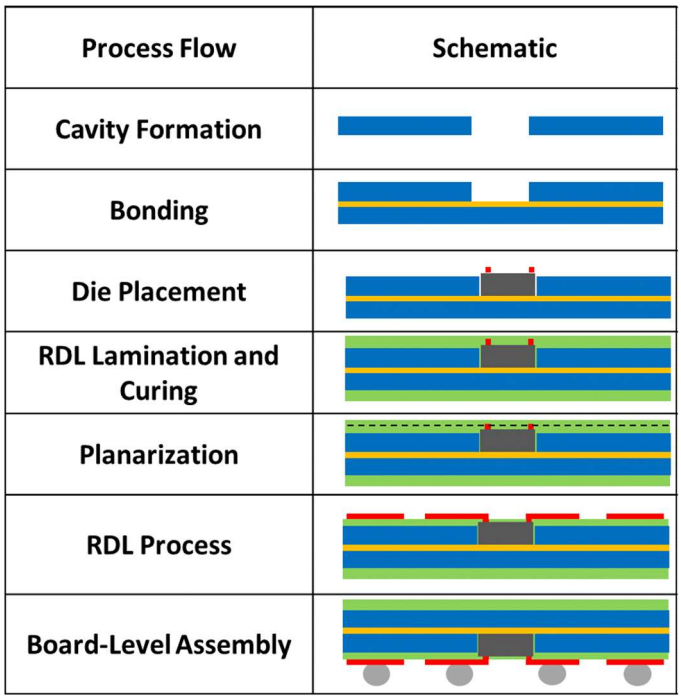



**Figure 40: Process flow of GPE packages with through cavity**

4.1.2.1.2 Fabrication

Glass cavity formation is the first step of the fabrication. Precise cavity formation in glass can be realized by various methods, including laser ablation, wet etching, mechanical dicing, sand blasting, ultrasound machining or by the direct use of photo-sensitive glass, as shown in Figure 411.

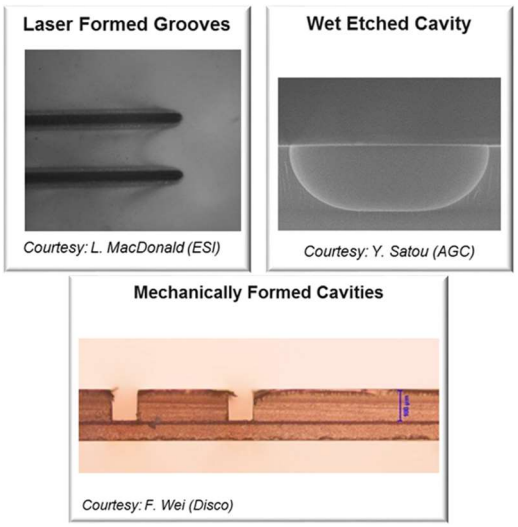



**Figure 41: Glass-cavity cross-section from various fabrication methods**

Figure 422 (a) shows the design of glass panels (panel size: 300 mm × 300 mm) with a thickness of 70 µm, and 26 through glass cavities in each panel. The cavities were formed using a combination of laser ablation and mechanical dicing. The top view of the fabricated glass cavity panel is shown in Figure 4242 (b), with cavity location and dimensional accuracy below +5 µm.

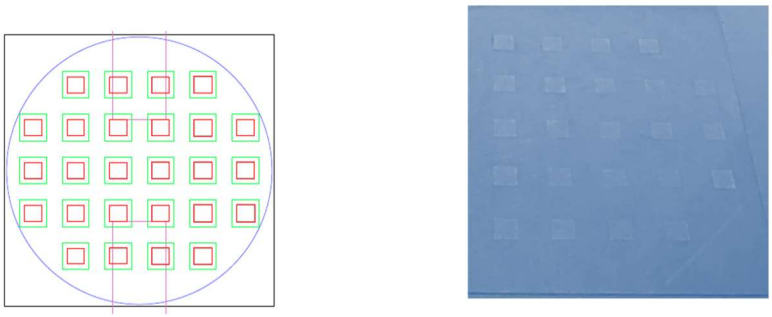



**Figure 42: Top view of glass cavity panel (a) designed, (b) fabricated**

The glass-cavity layer was then bonded to a 50 µm thick glass panel carrier with dry film adhesive. After the glass cavity is bonded on the glass carrier, the chips were placed into the

cavity. Daisy-chain test dies provided by Intel were used to emulate the embedded devices. The key characteristics of the die are: size - 6.469 mm × 5.902 mm, thickness - 75 µm, pad pitch 65 µm, and a Cu bump with the thickness of 20 µm. The top right corner of Intel test die is shown in Figure 4343.

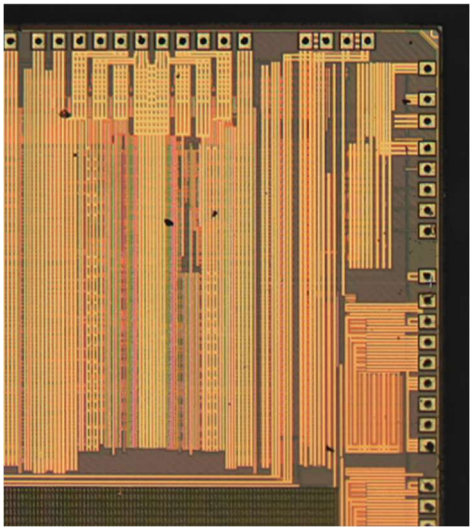


**Figure 43: Optical image of the top right corner of Intel Test Chip**

The effect of different die placement conditions such as temperature, tool size and force were investigated and optimized.

The optimized die-placement conditions such as bonding force, temperature and cycle time were determined and then applied to the assembly process in the glass cavities. Figure 4444 (a) shows the die placement process and Figure 4444 (b) shows the dies embedded in glass cavities after die placement.

**(a)** **(b)**

**Figure 44: (a) Die placement in glass cavities; (b) Optical image of embedded dies in the cavities**

After the dies were placed in glass cavities, RDL polymers were then laminated onto both sides and cured to minimize the warpage of the ultra-thin package. Figure 45 shows the top view of the GPE package after polymer lamination.

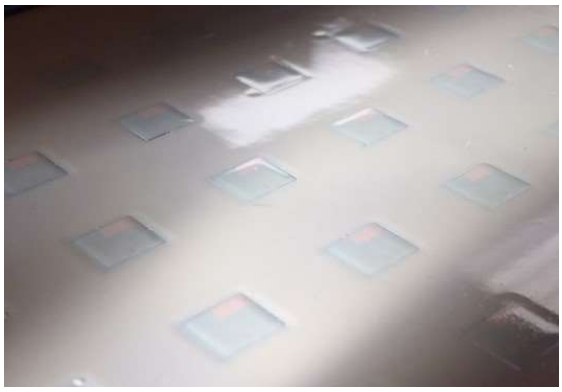


**Figure 45: Top view of GPE package after polymer lamination**

After polymer lamination and curing, a surface planarization tool from Disco was then used to planarize the surface of the panel and expose the copper micro-bumps on the die. A smooth surface of the Cu bump was observed after planarization, as shown in Figure 46.

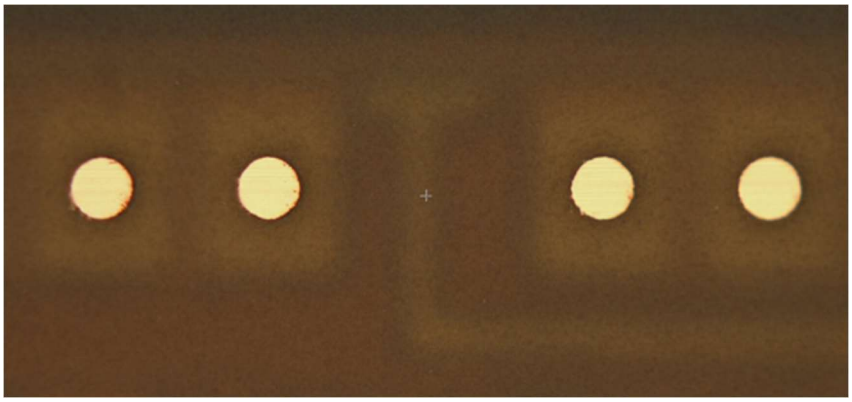


**Figure 46: Top view of GPE package after planarization**

Following the planarization process, a standard semi-additive process (SAP) was applied for patterning the Cu trace connected to the planarized Cu bump. The cross-section of the GPE package is shown in Figure 4747. The total thickness of the GPE package is 213.8 µm, including a 50 µm thick glass carrier, a 70 µm thick glass cavity panel, 75 µm thick test chips embedded in the glass cavity, the bonding dry film and the double-side RDL polymers.

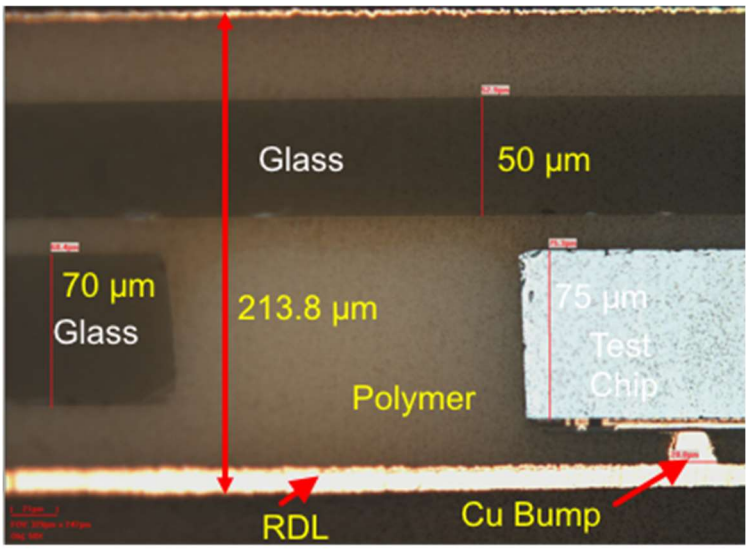
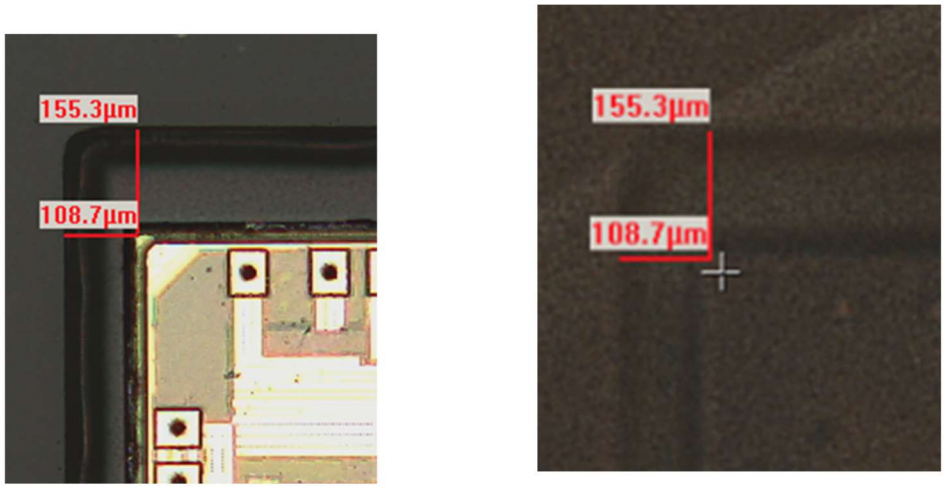



**Figure 47: Cross-section of a Glass Panel Embedding (GPE) Package**

Compared to other fan-out packages, GPE packages are ultra-thin, with thickness less than 215 μm which is a key advantage of GPE where there is no need for grinding at all. Furthermore, unlike high-density fan-out packages that require an organic package to connect to boards for large body sizes [22], GPE packages are designed to be directly-SMT attached to the board, enabled by the tailorability of the CTE of the glass panels and all the compliant interconnections. Lastly, the ultra-smooth surface and high dimensional stability of glass enables silicon-like RDL capability on large panels, with the potential of 1-2 μm critical dimensions (CD) [23] for high density fan-out applications.

4.1.2.1.3 Die-shift characterization

Did shift measurements are very critical in embedded fan-out technologies as a large value of the die shift would have severe impact on incorporating multiple dies in the package. The die shift is measured as the x, y distances between the die corner and the glass cavity corner before and after polymer lamination and curing. The die-shift comparisons are shown in Figure 48. Less than 5 μm die-shifts were observed among all the 52 dies that were characterized.




(a) (b)

**Figure 48: Top view of top left corner (a) after die placement, and (b) after polymer lamination and curing**

4.1.2.2 Demonstration of GPE packages with blind glass cavities

GPE packages with through cavities have been demonstrated as shown in previous chapter. However, the process is limited to the chips with bumps since a planarization process is needed to expose the copper micro-bumps on the die and connect it to the RDL layer. In this section, the microvia drilling process was demonstrated for the first time using a UV laser ablated via to interconnect the chip to the RDL layer which can also be applied to unbumped die such as the SiGe chips developed for the RADAR module.

4.1.2.2.1 Process flow

Figure 4949 shows the process flow of GPE package with blind cavities including the microvia drilling process. Glass cavities were first fabricated, and the dies were then placed into the glass cavities using a die attach film material from Nitto Denko Corporation. RDL polymers were then laminated and cured on both sides of the glass substrate to minimize

the warpage of the ultra-thin package. Microvias were then drilled using a Electro Scientific Industries, Inc. (ESI) UV laser tool on the chip pads, followed by a standard semi-additive process (SAP) for the fan-out RDL layer.

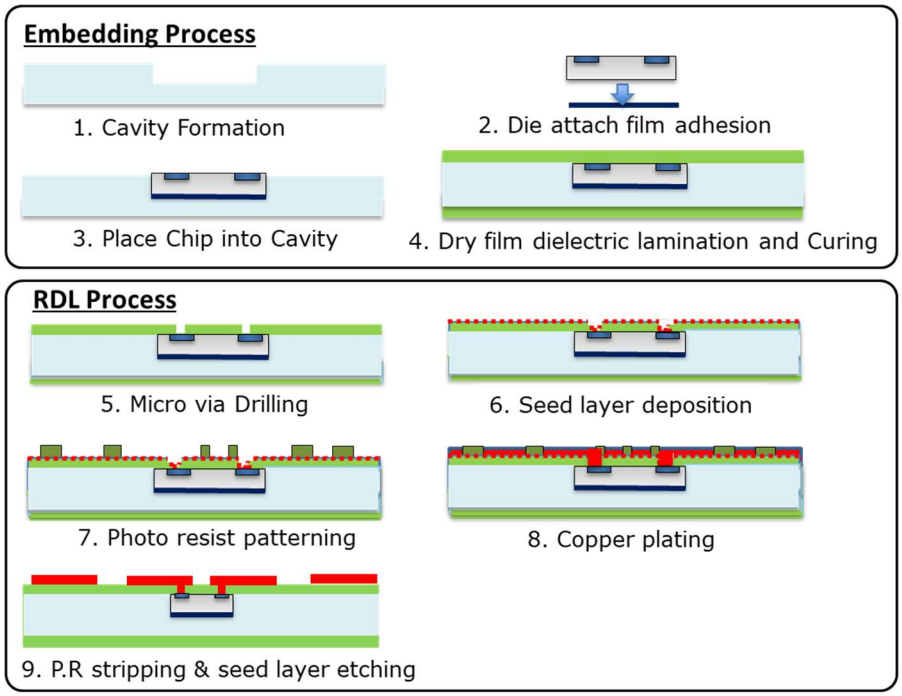



**Figure 49: Process flow of GPE packages with blind cavity**

4.1.2.2.2 Fabrication and die-shift characterization

For GPE packages with blind cavities, die attach films are needed in the die placement process.

Figure **50**50 shows the die attach film adhesion process and Figure 5151 shows the glass cavity panel after die placement using die attach film.

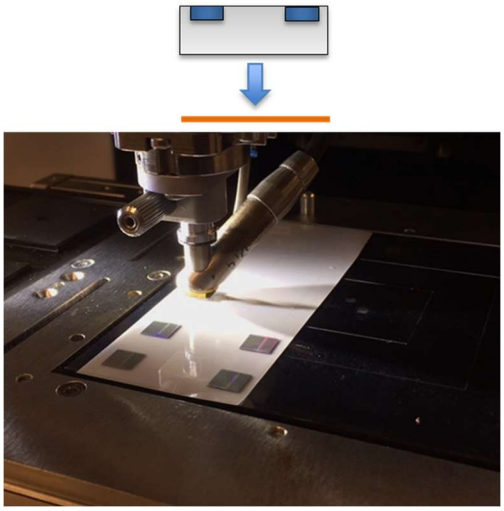


**Figure 50: Die attach film adhesion**

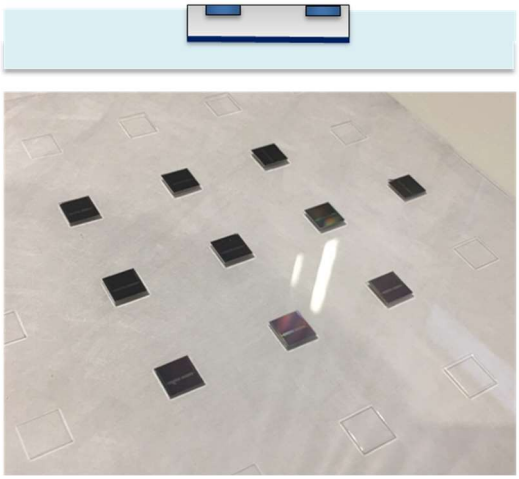


**Figure 51: Die placement in glass cavities with die attach film**

The die shift was characterized after curing, as shown in Figure 5252. The die shifts of 9 dies were shown, with the blue bar representing the die shift in x-direction and the red bar representing the die shift in y-direction. The average die shift is less than 2 μm. With reduced die shift, the size of the pads in the RDL layer on top of the chip I/Os can be designed smaller for the interconnection between chip and package. The reduced pad size

can minimize the parasitic effect of the pad and help solve the signal discontinuities of the chip interconnections at high frequencies for RADAR applications [7].

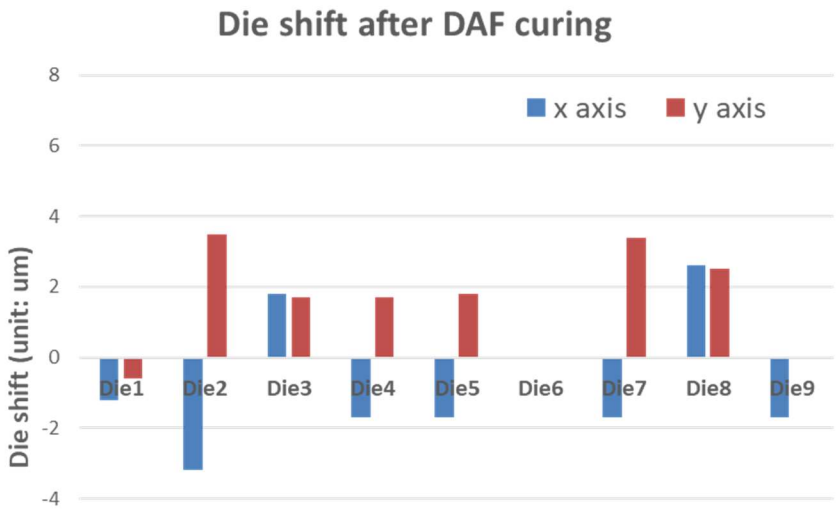



**Figure 52: Die shift after die attach film curing**

After the dies were embedded in the GPE package with die attach film and then covered with dielectric layers, microvias were drilled using a laser drilling tool from ESI to connect the chip to the RDL layer.

The microvia drilling process was first demonstrated on microvia drilling test chips with I/Os at 40 µm pitch. The test chips have no bumps but 10 µm diameter passivation openings on top of the I/Os. As shown in Figure 16, microvias with ~20 µm diameter were drilled to connect the 10 µm passivation opening on the die with good alignment and via size control, as shown in Figure 5353.

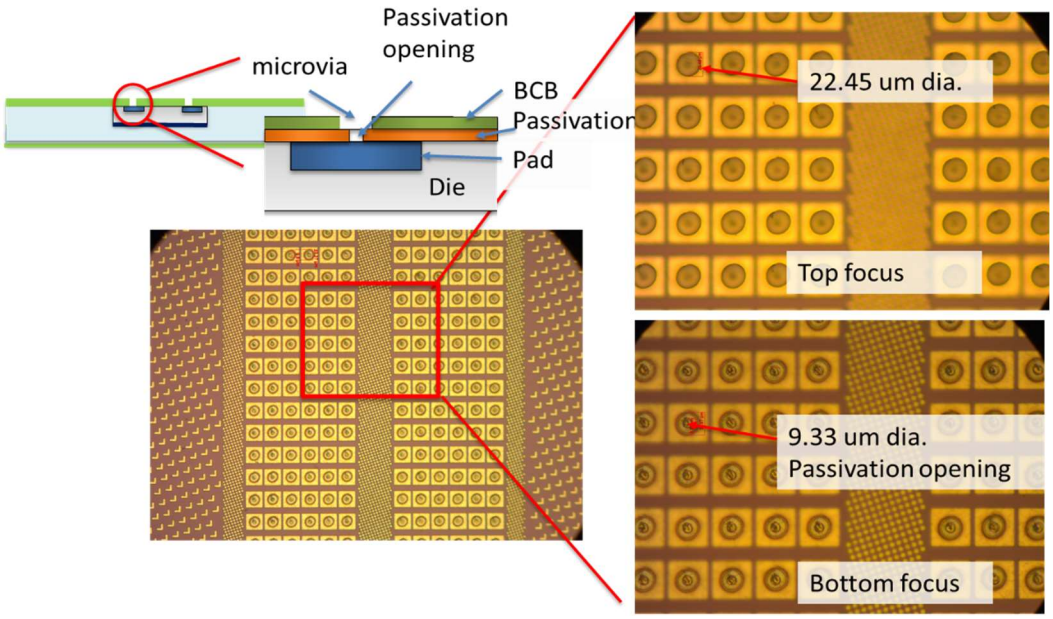



**Figure 53: Microvia drilling using UV laser**

The precise microvia drilling enables more microvias at finer pitch to connect the separate ground layers. The high microvia position accuracy can also reduce the size of pads on top of the embedded die I/Os for the signal transmission, which will reduce the parasitic effect and provide low loss interconnections.

### *4.1.3 Demonstration of ultra-thin GPE packages*

#### 4.1.3.1 Initial Process flow and demonstration

To further reduce package thickness, the ultra-thin GPE packages were proposed with the removal of glass carrier layer. The initial process is shown in Figure 5454.

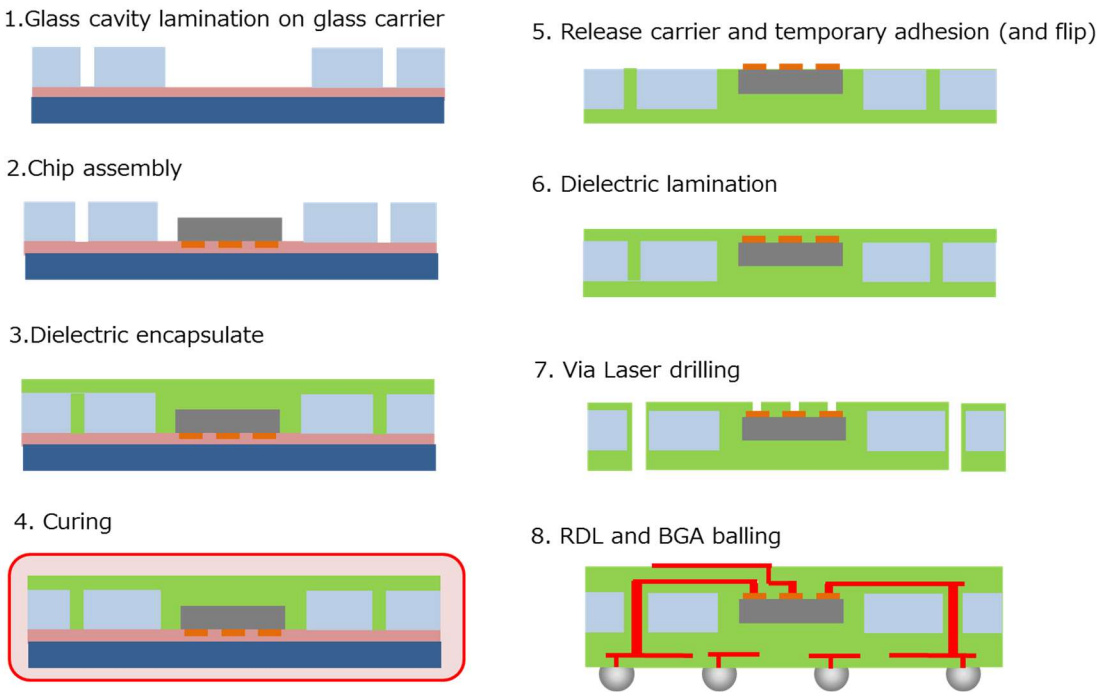



**Figure 54: Initial process flow for ultra-thin GPE packages**

As shown in Figure 5555, the face-up ultra-thin GPE package with dielectric was demonstrated, and the planarity of the dielectrics on top of the die area was characterized after carrier removal. Good chip-package planarity was observed with only 2 µm dielectric dimple depth, as shown in Figure 5656.

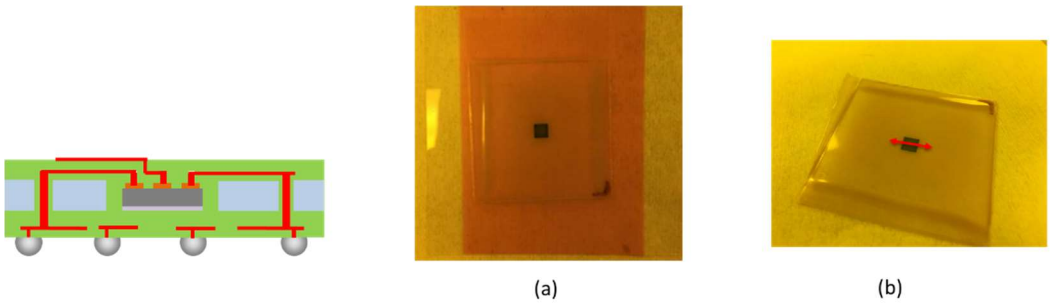



**Figure 55. Ultra-thin GPE after (a) die assembly and dielectric lamination, (b) glass carrier removal**

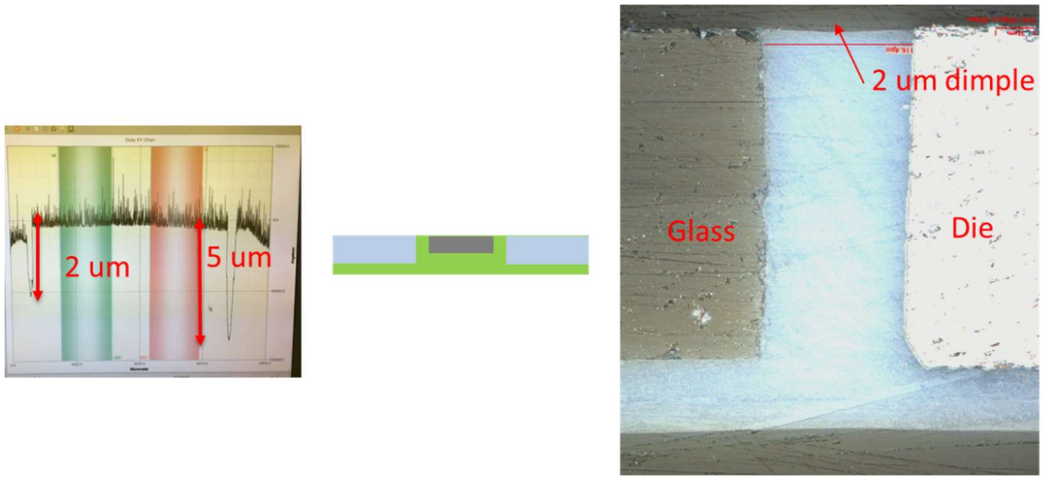



**Figure 56: Planarity measurement of an ultra-thin GPE package**

4.1.3.2 Warpage optimization and optimized process flow

The ultra-thin GPE process was first studied applying 300 µm thick glass cavity, and then further reduced to 100 µm thick glass cavity. A large warpage over 700 µm was observed after thermal releasing of the glass carrier and temporary bonding film (the 5th process in Figure 54) with 100 µm thick glass cavity, as shown in Figure 5757.

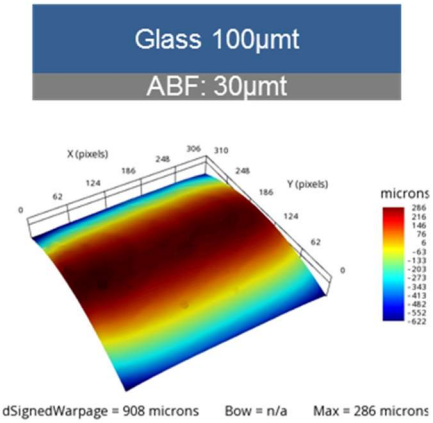



**Figure 57: Warpage measurement of ultra-thin GPE packages**

A double side carrier process was then proposed to optimize the warpage, as shown in Figure 5858.

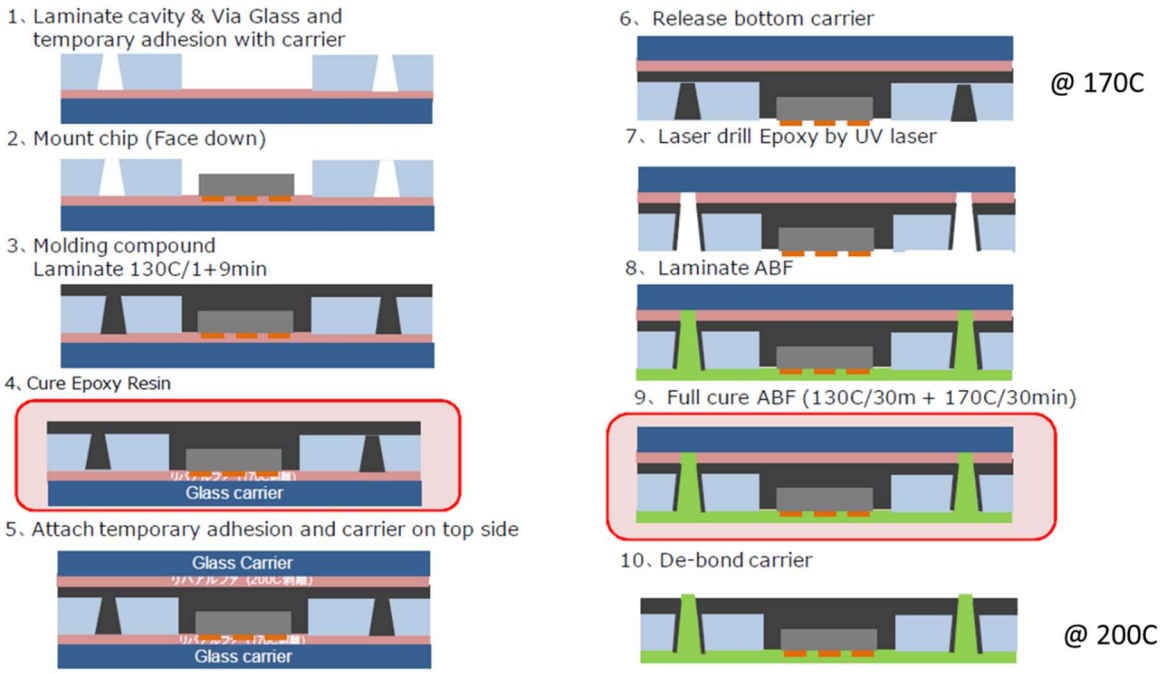



**Figure 58: Double side carrier process of ultra-thin GPE packages for warpage reduction**

The measured warpage of the ultra-thin GPE package, shown in Figure 59, can be reduced to less than 80 µm over a 2 inch panel upon applying the optimized double side process.

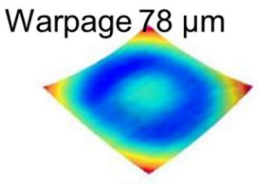



**Figure 59: Warpage measurement of ultra-thin GPE package applying the double side process**

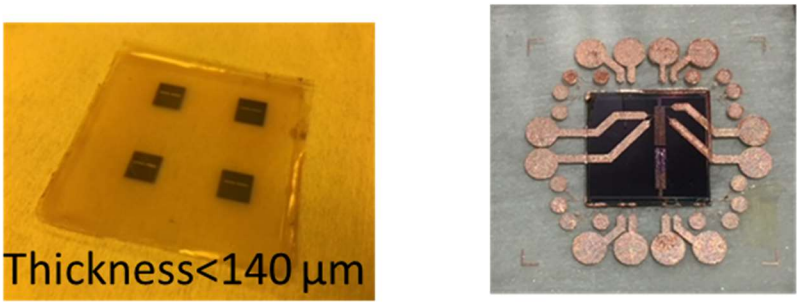
## 4.2 Demonstration of GPE package with minimum package thickness and low system loss

### *4.2.1 Demonstration of GPE package with minimum package thickness*

The ultra-thin GPE packages were demonstrated applying the optimized double side carrier process with the detailed specifications shown in Table 1111. The demonstrated ultra-thin GPE package is shown in Figure 6060, with thickness less than 140 µm. The warpage measured was less than 80 µm over a 2 inch panel upon applying the optimized double side process.

**Table 11: Specifications of ultra-thin GPE package fabrication**

| Parameter | Value |
|---|---|
| Glass cavity thickness | 100 um |
| Glass carrier thickness | 1 mm |
| ABF thickness | 30 um |
| Die thickness | 100 um |
| Die size | 7.2 mm x 7.2 mm |
| Temporary bonding film thickness | 10 um |
| Temporary bonding film A release temp. | 170 C |
| Temporary bonding film B release temp. | 200 C |




(a) (b)

**Figure 60: Ultra-thin GPE package: (a) after carrier removal, (b) after RDL process**

### *4.2.2 Demonstration of GPE package with low package loss*

#### 4.2.2.1 Die-package Co-design

In this section, a die-package codesign was proposed for high-precision, high-frequency characterization of ultra-thin GPE package for RADAR applications.

A low noise amplifier (LNA) was designed applying the 77 GHz SiGe technologies by Prof. John Cressler's team from Georgia Tech. A two-stage differential cascode topology is chosen for the preliminary LNA design as shown in Figure 6161. Inter-stage matching is realized using a transformer for compact form-factor. The center-taps of the transformer coils are used to supply bias. Transformer-based baluns are included in the design for single-ended on-chip circuit characterization.

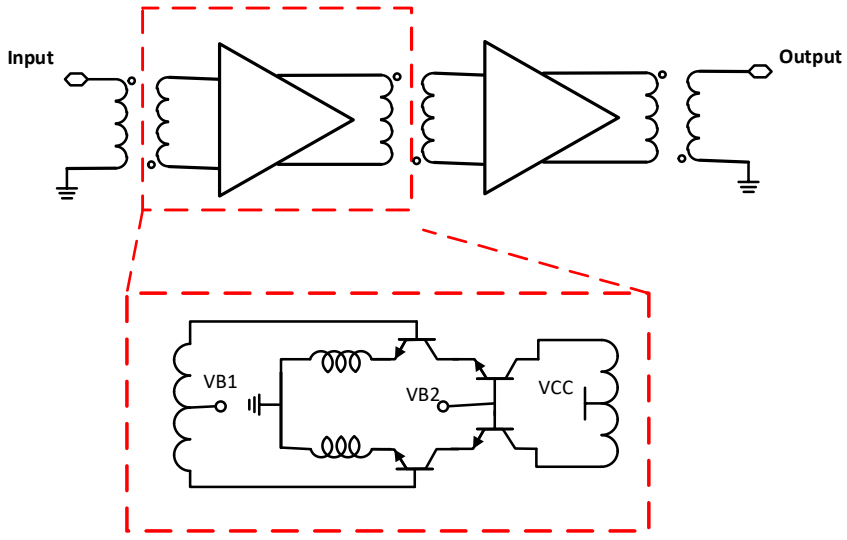



**Figure 61: Block diagram of the 2-stage LNA with transformer balun and inter-stage matching**

The layout of the two-stage LNA is shown in Figure 6262. The design adopts a pseudo-differential topology. The base nodes of the cascode transistors are placed closely in the design with a by-pass shunt capacitor for stability. All three biases (VCC, lower base bias and cascode base bias) of each stage are supplied via bond pads for more testing flexibility. The design occupies 0.61 × 0.97 $mm^2$ chip area including bond pads. The LNA design shows a simulated gain (S21) of 18.125 dB with a 3 dB bandwidth of 8.3 GHz from 74.9 GHz to 83.2 GHz, and a return loss (S11) of -1.2 dB at 77GHz, as shown in Figure 6363.

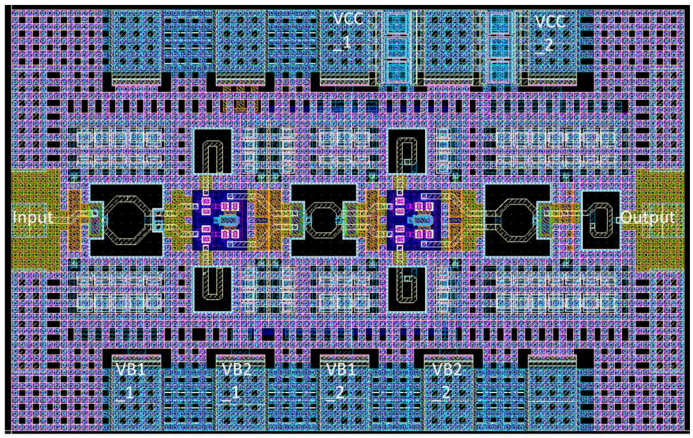



**Figure 62: Layout view of the two-stage LNA design**

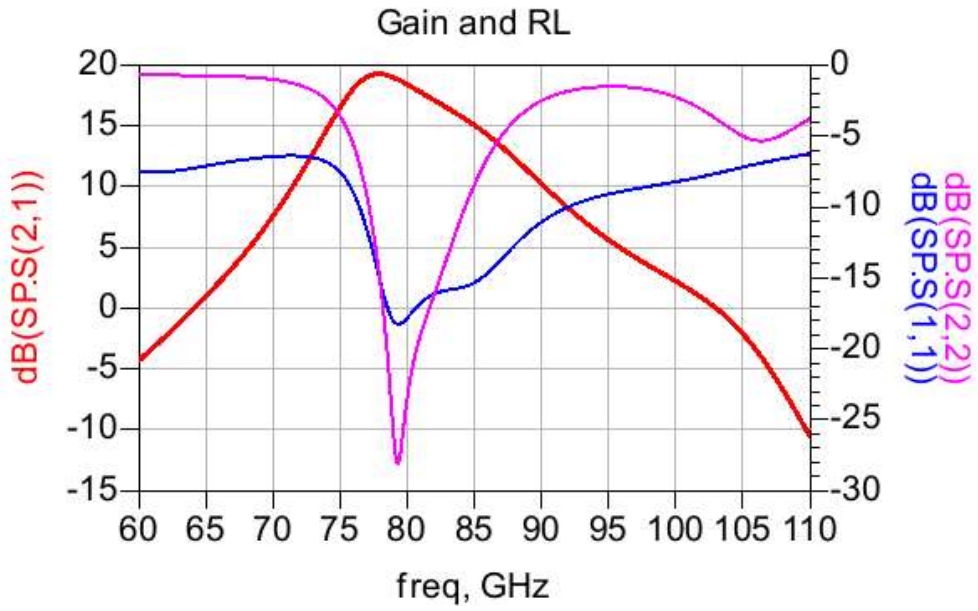



**Figure 63: Simulated gain and return loss of the LNA.**

A package design is proposed based on the chip design layout, as shown in Figure 6464.

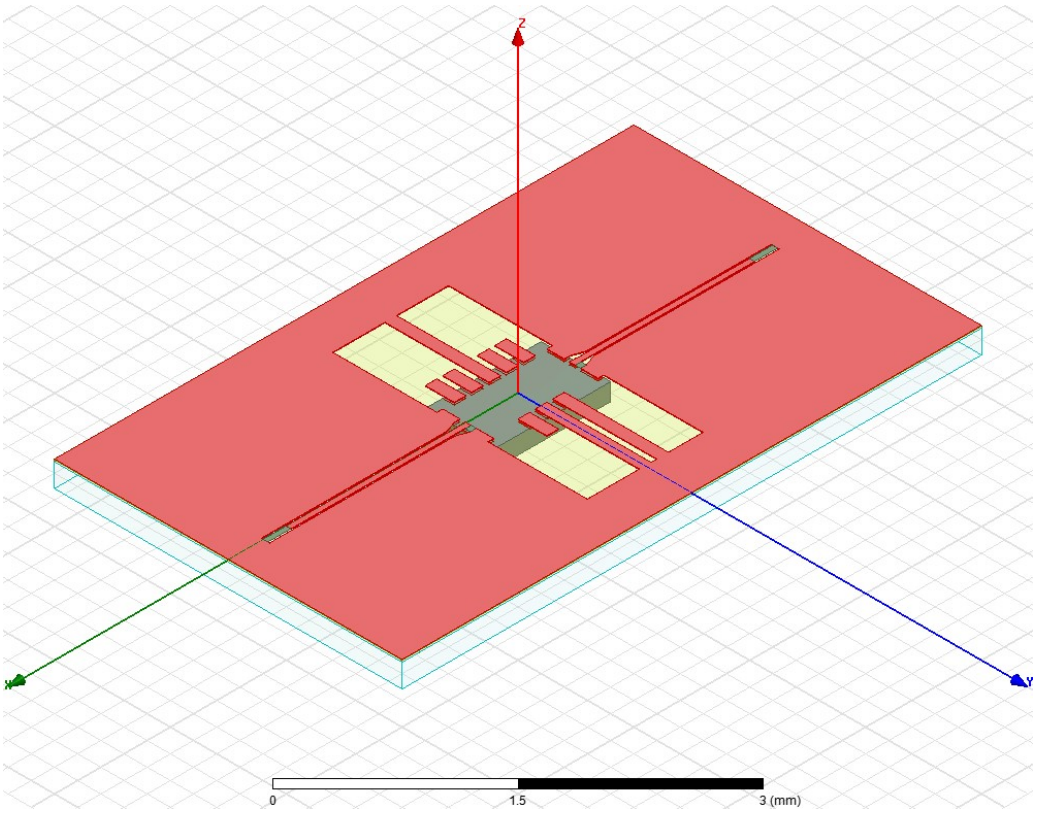



**Figure 64: Package design for RADAR module with LNA chip.**

4.2.2.2 Characterization of insertion and return loss

Figure 65 shows the characterized results of the insertion and return loss of the LNA after embedded in the ultra-thin GPE package. After de-embedding, the insertion loss (S21) of the ultra-thin GPE package is -0.6 dB, and the return loss (S11) is - 12.8 dB at 77GHz, both achieved less loss than the prior-art (eWLB, shown in Figure 11): insertion loss as low as −0.65 dB and a return loss below −16 dB at 77 GHz [21].

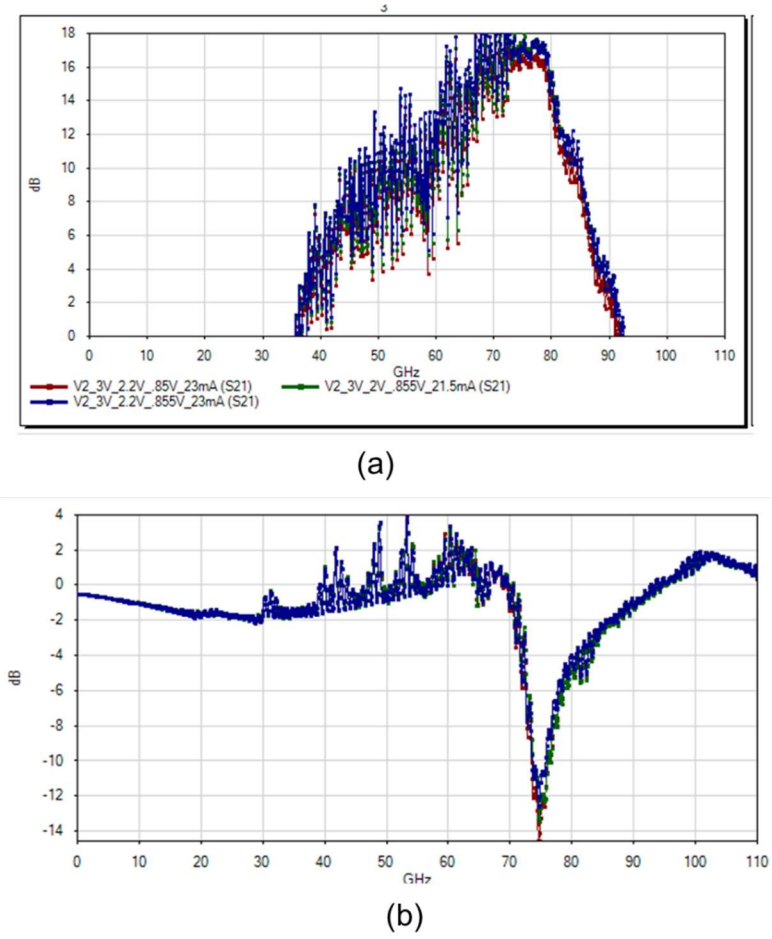



**Figure 65: Measured (a) insertion loss (S21) and (b) return loss (S11) of the LNA after embedded in the ultra-thin GPE package.**

4.2.2.3 Characterization of noise figure

The noise figure of a LNA can be calculated using the equation as below:

$$NF = 10log_{10}\left[1 + \frac{R_{LG}}{R_S} + \frac{R_{GATE,eq}}{R_S} + \gamma g_{d0} R_S \left(\frac{\omega}{\omega_T}^2\right)\right] \quad (1)$$

The second, third, and fourth terms in square brackets of (1) represent parasitic resistance of the gate inductor, gate resistance of the MOS transistor, and drain current noise of the MOS transistor, respectively. The inductor can be improved by ultra-thin GPE package

compared with the on-chip inductor. Based on Table 12, by applying ultra-thin GPE package, both Q factor and parasitic resistance can be improved three times.

**Table 12. Inductance, parasitic resistance and quality factor of on-chip and ultra-thin GPE packages.**

| | On-chip | GPE |
|---|---|---|
| Inductance (nH) | 2.91 | 2.85 |
| Parasitic Resistance (Ω) | 8.57 | 2.82 |
| Quality Factor | 11.1 | 34.0 |

The characterized noise figure of the LNA is shown in Figure 666. The noise figure improves to 2.95 dB with the ultra-thin GPE inductor (from 3.45 dB for the on-chip version) at the target operation frequency of 77GHz.

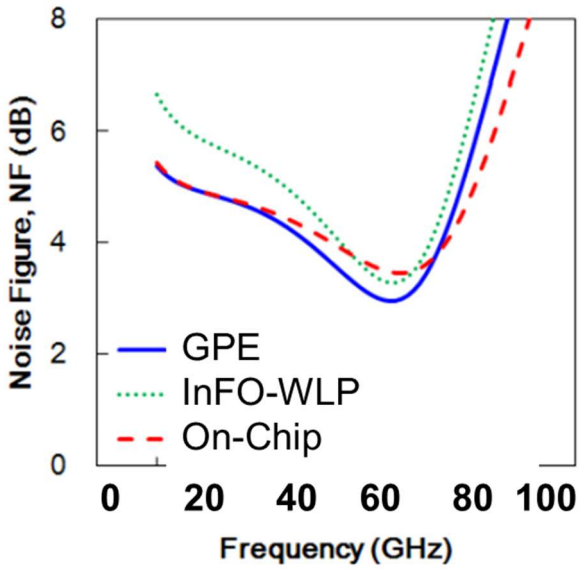



**Figure 66. Noise figure with GPE inductor, on-chip inductor, and FO-WLP inductor.**

# CHAPTER 5. KEY TECHINICAL ACCOMPLISHMENTS

## 5.1 Research Summary

The objectives of the proposed research are to model, design, fabricate and demonstrate ultra-thin and high-performance 3De Glass Panel Embedded (GPE) packages for mmWave applications with minimal interconnect loss.

Two specific goals were defined in this research:

1) Modeling and design of 3D GPE package with minimum package thickness and high electrical performance which includes a) low transmission line loss, b) system insertion loss and c) TPV loss.
2) Fabrication and demonstration of 3D GPE package with high precision RDL, low warpage, minimized package thickness and high electrical performance.

To achieve these objectives, the following two main research challenges are identified in 1) modeling and design and 2) fabrication and demonstration of 3D GPE packages. In modeling and design, one key challenge is to achieve minimal package height. The other challenge in modeling and design of GPE package for high electrical performance is the electrical discontinuities in die-to-package interconnections. Such an impedance discontinuity generates reflections, resulting in time-domain signal degeneration. In the fabrication of GPE packages, warpage and precise process control of RDL are the two main challenges. In the demonstration of GPE packages with ultra-thin glass, handling and warpage are critical.

To address these challenges, two main research tasks were proposed and carried out: Task 1a) is to design package architecture for minimum package thickness. Task 1b) is to model

and design embedded chip interconnections with minimum loss. This task contains several sub-tasks including modeling of transmission lines on GPE packages; design and modeling of interconnections; and modeling of package loss for ultra-thin GPE packages. Task 2a) is to fabricate GPE packages with high-precision process control and low warpage. Task 2b) is to demonstrate GPE packages with minimum package thickness and low system loss & low noise figure.

For task 1a), GPE package architecture with through glass cavity and backside glass carrier was designed with thickness less than 250 μm. A thinner GPE architecture was also designed with thickness less than 150 μm by removing the glass carrier. For task 1b), the transmission-line on GPE package was modeled with the minimum insertion loss to be 0.140 dB/mm at 77 GHz enabled by ultra-low loss dielectrics; the low-loss interconnects were designed and modeled with interconnection loss below 0.12 dB at 77GHz; the loss for the whole GPE package (including transmission-line, TPV and interconnection) was modeled to be less than 0.5 dB. For task 2a), GPE package with high-precision process control was fabricated including: 2-5 μm die shift, good chip-to-package planarity with dimple < 2 μm, and high precision microvia drilling. The warpage of ultra-thin GPE package was reduced to < 80 μm over a 2inch panel applying double carrier process. For task 2b), an ultra-thin GPE package with thickness less than 140 μm was demonstrated by applying advanced low-cost large panel, double side carrier processes; low LNA noise figure was characterized to be 2.95 dB with GPE inductor compared to 3.45 dB with FO-WLP at 5.2 GHz.

## 5.2 Research Novelty

The novelty of the research presented in this thesis include: (a) first time demonstration of ultra-thin, low-warpage and low die-shift GPE packages with thickness of less than 150

μm. This required development of advanced low-cost large panel, double-side carrier and embedding processes which were developed as part of this thesis work; (b) design and modeling of low-loss interconnects with interconnection loss below 0.2 dB at 77 GHz, enabled by ultra-low loss RDL dielectric, and optimized high precision processes for via drilling and photolithography with minimal variations in line and via geometries on glass substrates; (c) demonstration of glass panel embedded (GPE) packages with low system insertion loss (0.6 dB @ 77 GHz) & low noise figure (2.9 dB @ 77 GHz), enabled by chip-package co-design and GPE architecture.

- The research work reported in this dissertation as compared to the prior art on fan-out wafer-level package (FO-WLP) is as follows:

  Ultra-thin GPE packages were designed and demonstrated as a superior solution for mm-Wave applications with the lowest package thickness and lowest interconnection loss compared with previous wafer-level fan-out solutions. This required advances in designs, materials, processes, and integration of all these into cross-disciplinary test vehicles. The advantages of ultra-thin GPE package compared to FO-WLP approaches are listed in the Table 13 below.

  - Materials: glass as the substrate material with suitable CTE (made feasible owing to the tailorablity of glass CTE, between 3.8 to 9 ppm/ºK) to reduce the mismatch with chips and superior dimensional stability; ultra-thin and low-loss dielectrics with loss tangent below 0.001.
  - Processes: precise glass cavity formation; double carrier process for low warpage; precise microvia drilling for low loss interconnects.

- Mechanical performance: warpage less than 80 µm over a 2 inch glass panel; die-shift less than 5 µm.
- Electrical performance: Package insertion loss of less than 0.5 dB.
- Cost: large panel processing at lower cost.

**Table 13: Comparison between FO-WLP and GPE.**

| Properties | | FO-WLPs | GPE |
|---|---|---|---|
| Materials | Substrate | Molding compound | Glass |
| | Dielectric | Loss tangent < 0.1 | Loss tangent < 0.001 |
| | CTE | CTE 30-50 ppm/°C | CTE 3.8-9 ppm/°C |
| Processes | RDL | Back end of line (BEOL) Less than 1 µm L/S | SAP 2 µm L/S |
| | Through package via (TPV) | Through mold via (TMV) dia. 100 µm, pitch 200 µm | Through glass via (TGV) dia. 20 µm, pitch 40 µm |
| Test vehicle Characteristics | Warpage | > 500 µm on 6inch wafer | less than 80 µm over a 2 inch panel |
| | Die-shift | >10 µm | 2-5 µm |
| | Thickness | 300 -500 µm | <150 µm |
| Electrical performance | Insertion loss | 0.8 dB | 0.2-0.5 dB |
| Relative Cost | | High (Wafer) | Low (Panel) |

- The research reported in this dissertation, as compared to the prior art on embedded silicon fan-out package (eSiFO), as shown in Figure 16 includes:
    - Smaller package height (< 150 μm) than eSiFO (200 μm)
    - No need for back grinding to achieve minimum package height, and thus lower cost.
    - Easier TPV formation and lower TPV loss (designed as part of this thesis work) than TSV loss for potential 3D integration.
- The research reported in this dissertation, as compared to the prior art on other glass-based substrate packages is as follows:

Glass-based substrate packages have been proposed and widely studied due to the superior property of glass itself including ultra-high resistivity, low electrical loss, low dielectric constant, adjustable coefficient of thermal expansion (CTE) in between Si and PWB board, and exceptional dimensional stability. Compared with other glass-based substrate packages, the main contributions of this research include:

- Architecture designs of ultra-thin GPE packages.
- First-time fabrication and demonstration of GPE package with total thickness less than 215 μm.
- First-time fabrication and demonstration of ultra-thin GPE package with total thickness less than 150 μm by applying double-side carrier process.
- Process development and optimization for: 1) Precise glass cavity formation, 2) hermetic and non-hermetic glass-to-glass bonding, 3) accurate die placement, 4) precise microvia drilling, 5) surface planarization and 6) warpage reduction.

- Design and modeling of low-loss interconnects in GPE packages with insertion loss below 0.2 dB at 77 GHz.
- Demonstration of GPE packages with low system insertion loss (-0.6 dB @ 77 GHz) & low noise figure (2.9 dB @ 77 GHz), enabled by advanced chip-package co-design, and low-loss GPE interconnections.

## 5.3 Publications

The published papers, book chapters and plan for future publications are listed in Table 14.

**Table 14: Published papers, book chapters and plan for future publications.**

| Publications | Submit Date |
|---|---|
| Co-author of a book chapter in "Fundamentals of Device and Systems Packaging: Technologies and Applications", McGraw Hill Professional | 2019 |
| Design, Demonstration and Characterization of Ultra-thin Low-warpage Glass BGA Packages for Smart Mobile Application Processor, IEEE ECTC | 2016 |
| First demonstration of panel glass fan-out (GFO) packages for high I/O density and high frequency multi-chip integration, IEEE ECTC | 2017 |
| Next Generation of Automotive Radar with Leading-Edge Advances in SiGe Devices and Glass Panel Embedding (GPE), IEEE ECTC | 2018 |

| | |
|---|---|
| Co-author of Design and demonstration of Glass Panel Embedding for 3D System Packages for heterogeneous integration application, Journal of Microelectronics and Electronic Packaging | 2019 |
| First Demonstration of Glass Panel Embedded Packages for High Frequency Applications, IEEE CPMT | January 2020 |
| Ultra-low-loss Interconnections in Glass Panel Embedded Packages for mmWave Applications, IEEE CPMT | Dec 2020 |
| Modeling, Design and Demonstration of Glass Panel Embedded mmWave Applications, IEEE CPMT | Jan 2021 |

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